

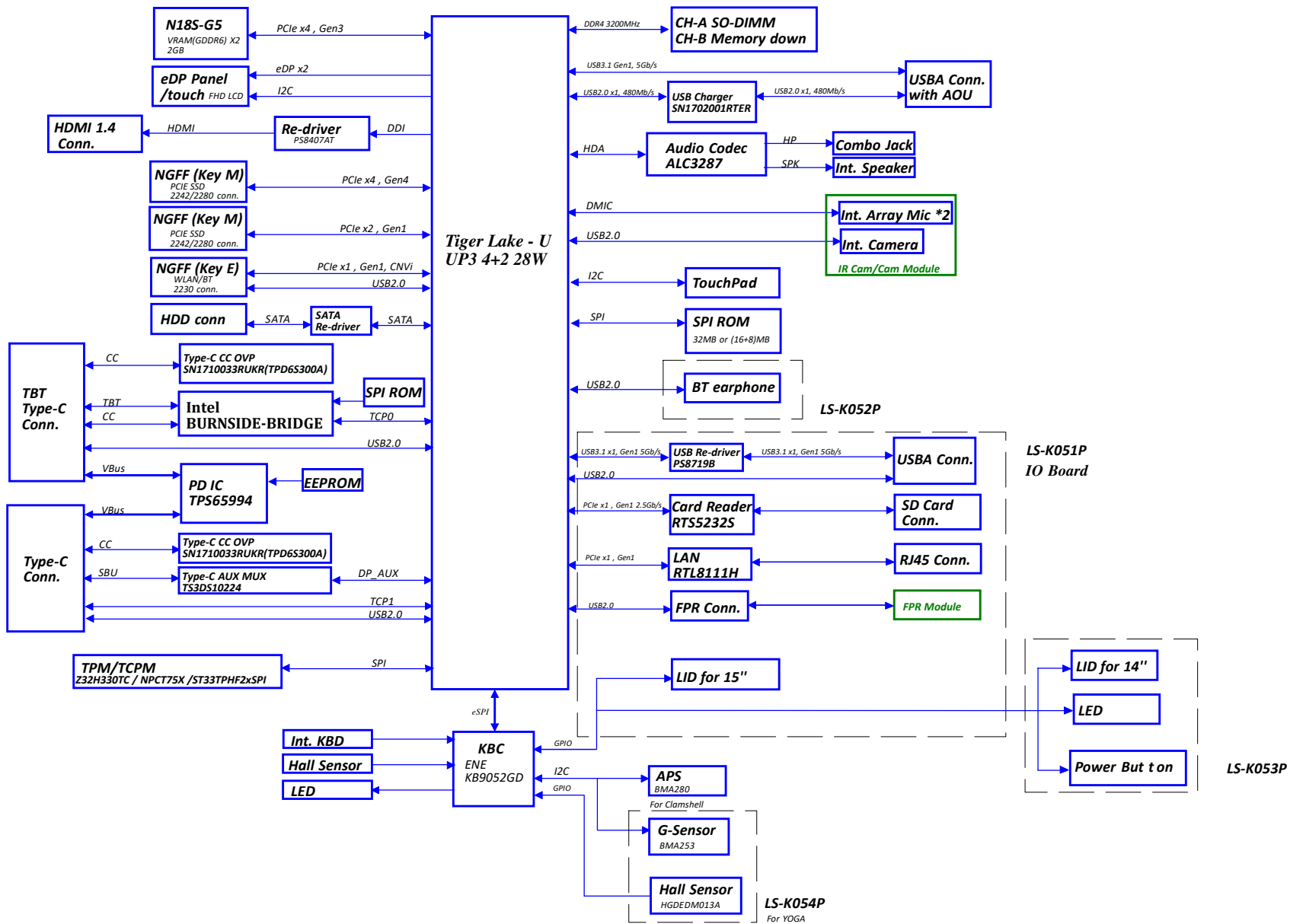
Compal LA-K051P

FLV34 GLV3Y MB Schematic Document

Rev: 1.A

2020.07.21

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BOM Structure Table

Funct i on	Stuf f	Un-Stuf f
dGPU SKU	DIS@	UMA@
dGPU support GC6	GC6@	NOGC6@
YOGA SKU	YOGA@	CLAHSHELL@
CLAMSHELL SKU	CLAHSHELL@	YOGA@
DDR DDP	DDP@	SDP@
DDR SDP	SDP@	DDP@
EMI / ESD / RF Components	EMI@ RF@ ESD@ BT_EMI@	@EMI@ @RF@ @ESD@
CNVI	CNVI@	RMT@
CMC	CMC@	
SPI ROM	16+8M@	32M@
USBA AOU	AOU@	NAOU@
TPM	TPM@ ST@ /Nuvton@/ Nat i ons @	NTPM@
GLITCH	GLITCH@	
KB Backlight	KBL@	
Touch Screen	TOUCH@	@TOUCH@
For Signal Test	MP@	
BT earphoen	BT@	
HDD	HDD@	@HDD@
Finger Print	FP@	NFP@
NC Components	@	
ME Cnector	ME@ CLIP@	
JUMP (HW & PWR)	JUMP@	@JUMP@

HSIO Port Table (CPU)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	PCle4 #0	SSD1	CLK0 & CLKREQ#0	PCle interface
1	PCle4 #1			
2	PCle4 #2			
3	PCle4 #3			

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	USB3.1 #1 / PCle #1	USB3.1 Type A Port 1 (MB)	NA	USB3.1 interface
1	USB3.1 #2 / PCle #2	USB3.1 Type A Port 2 (DB)	NA	USB3.1 interface
2	USB3.1 #3 / PCle #3	SSD2	CLK3 & CLKREQ#3	PCle interface
3	USB3.1 #4 / PCle #4			
4	PCle #5	dGPU	CLK4 & CLKREQ#4	PCle interface
5	PCle #6			
6	PCle #7			
7	PCle #8			
8	PCle #9	LAN	CLK1 & CLKREQ#1	PCle interface
9	PCle #10	Carder Reader	CLK2 & CLKREQ#2	PCle interface
10	PCle #11 /SATA0	HDD	NA	SATA interface
11	PCle #12 /SATA1	WLAN	CLK5 & CLKREQ#5	PCle interface

Power State

STATE	SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
S0IX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Load BOM Option Table

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

Load BOM Option Table for Baseline

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-A (MB)
2	USB Type-C (MB TBT)
3	USB Type-C (MB)
4	BT earphone
5	USB Type-A (DB)
6	NA
7	RGB Camera
8	NA
9	Finger print
10	NGFF WLAN+BT (KEY E)

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM	DIMM1	TBC	TBC	0xA0
		DIMM2	TBC	TBC	0xA4
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM	Re-Timer	TBC	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3V_PRIM	PD (CYPD5225)	0x08h	TBC	TBC
		PD (TI65988)	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SML1CLK EC_SML1DATA	+3VLP_EC				
		GPU	0x41	TBC	TBC
		THERMAL	0x4C	0X98	0x99
		PD (CYPD5225)	0x08h	TBC	TBC
		PD (TI65988)	TBC	0X46	0X47
				0X4E	0X4F

I2C Address Table (TBC)

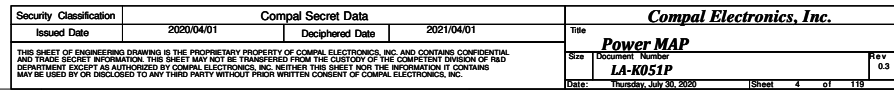
I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	+3VS	G-Sensor KXCJ9-1008	0x0FH	TBC	TBC
		ALS CM32181A3OP	0x48H	TBC	TBC
I2C 2	+3VS	HDMI2.0 Re-Timer	TBC	TBC	TBC
I2C 3	+3VS	Track Pad	0x2CH	TBC	TBC
ISH_I2C 0	+1.8VS	SENSOR_KMX61G (Reserve)	0FH	TBC	TBC

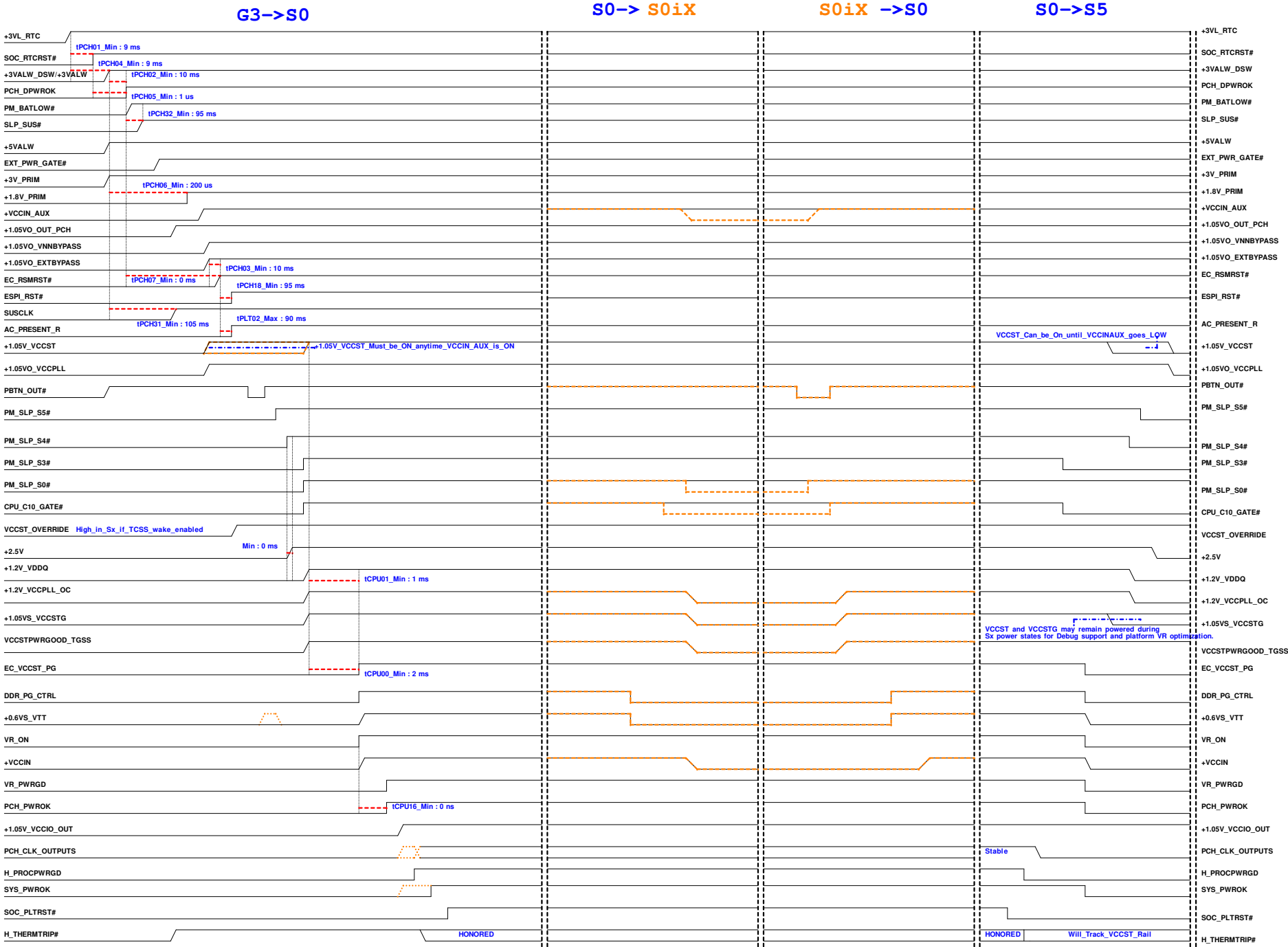
Voltage Rails

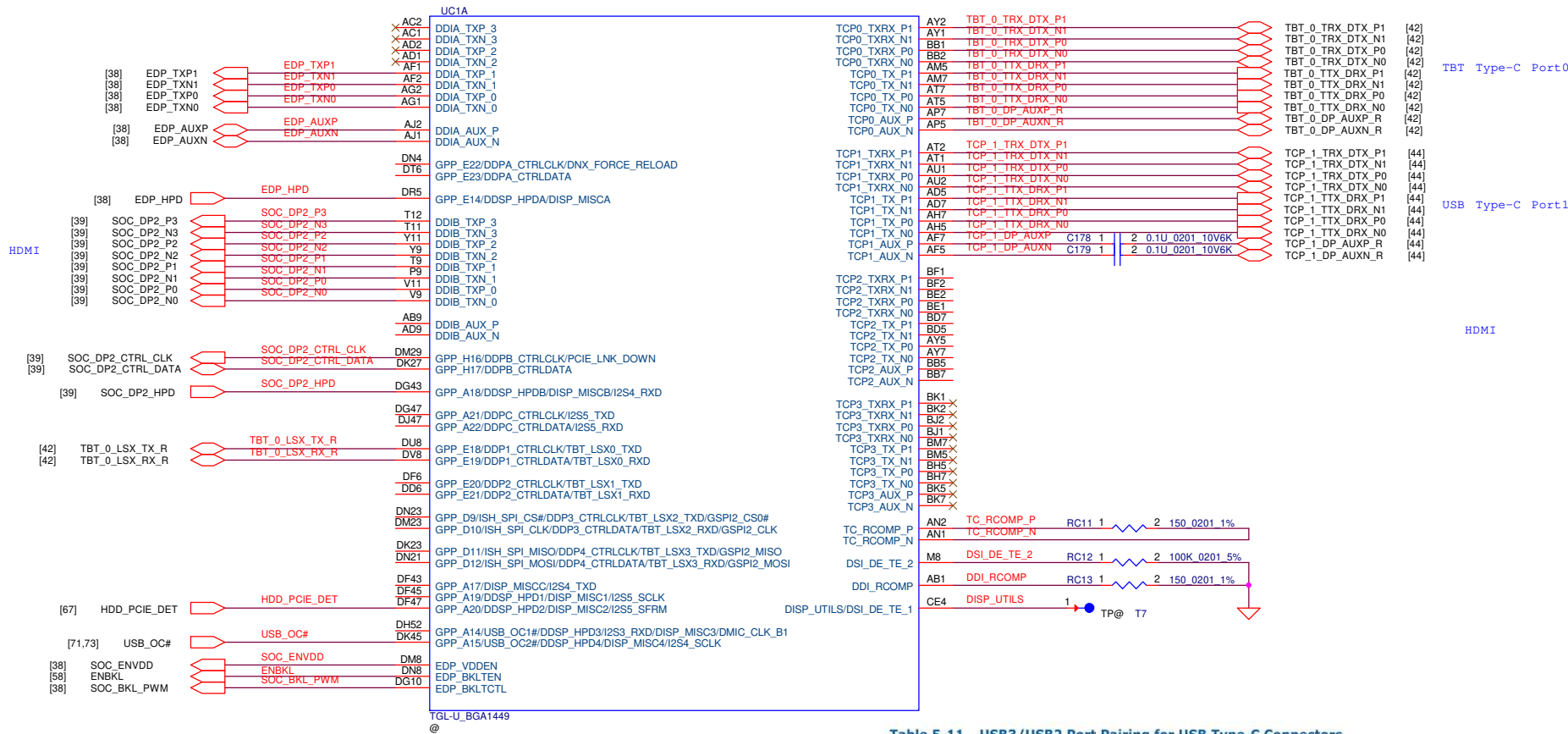
Power Plane	Descript i on	S0	S0ix	S3	S4/S5
+20V_ADP_IN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery po wer supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery po wer rai f or po wer drcut	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.0VS_DGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	ON	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

FOA01 Schematic: LA-H691PRO1_0401A



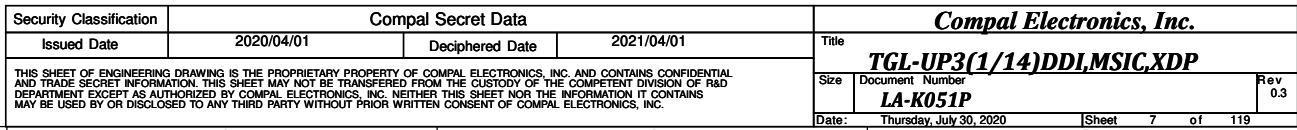




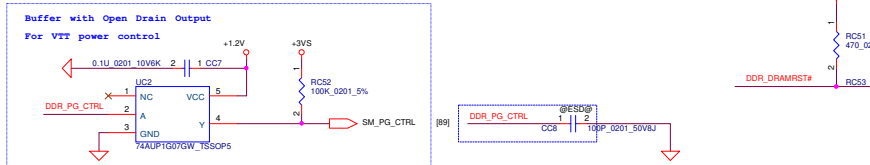
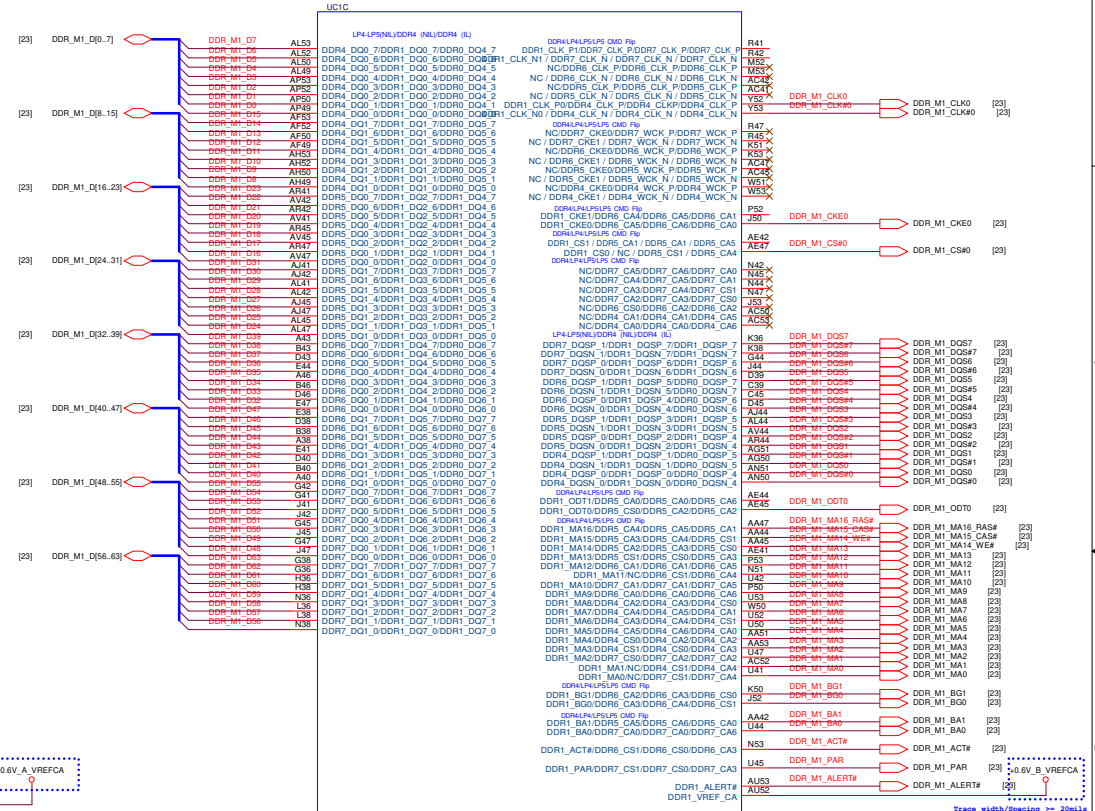
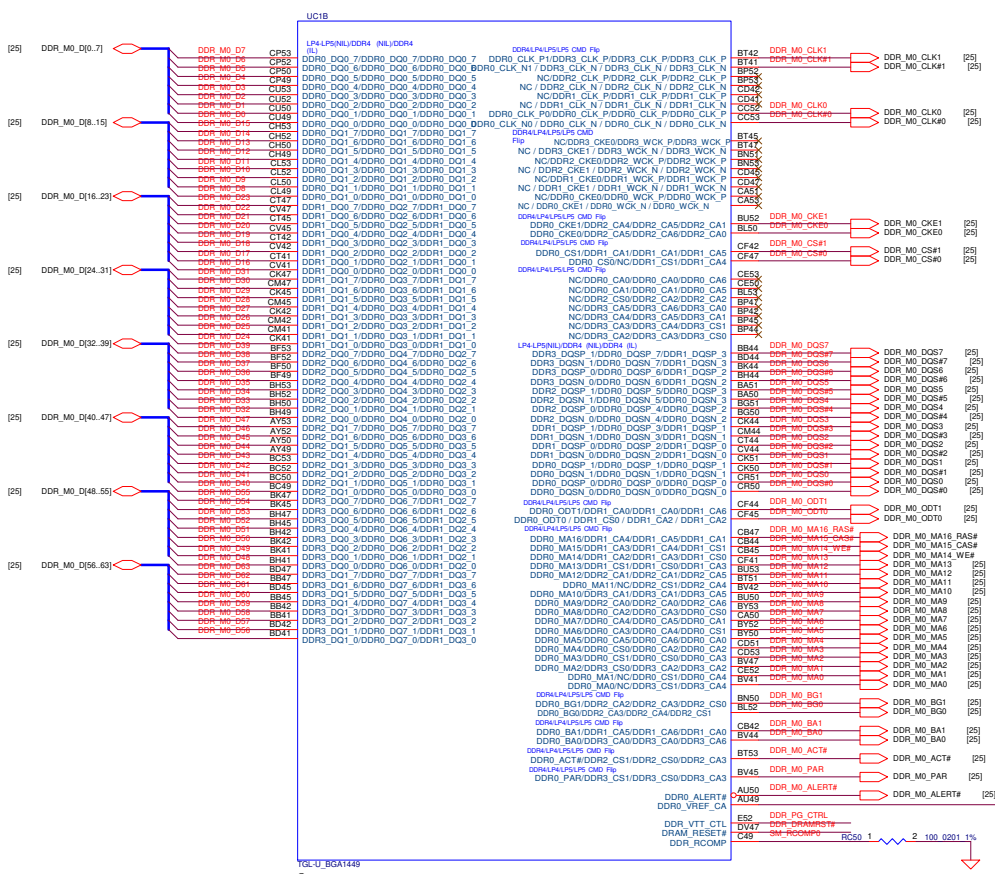
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

+3V_PRIM
 RC360 1 2 10K 0201 5% USB_OC#
 RC378 1 2 10K 0201 5% HDD_PCIE_DET
 RC21 1 2 100K 0201 5% SOC_ENVDD
 RC22 1 2 100K 0201 5% ENBKL
 +3V
 RC367 1 2 4.7K 0201 5%
 RC366 1 2 20K 0201 5%
 TBT_0_LSX_RX
 TBT_0_LSX_RX
 TBT_LSX #0 PINS VCCIO CONFIGURATION
 NO INTERNAL PU/PD
 HIGH: 3.3V
 LOW: 1.8V

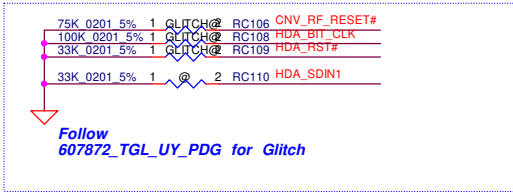
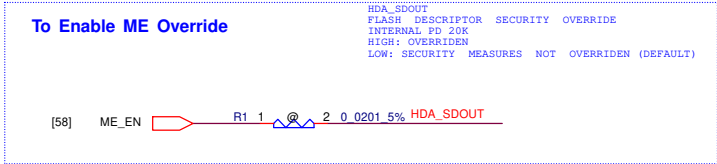
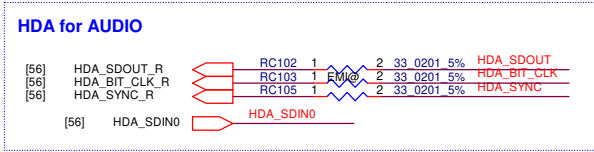
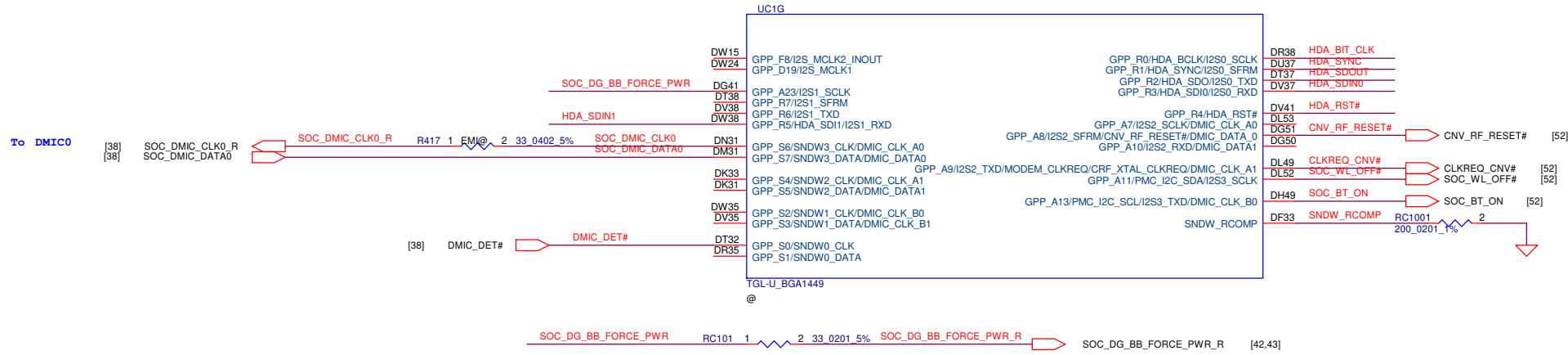
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Follow Intel DDR4 N1E

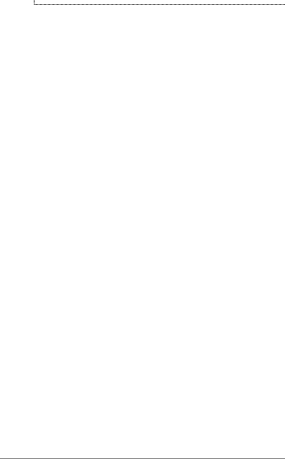
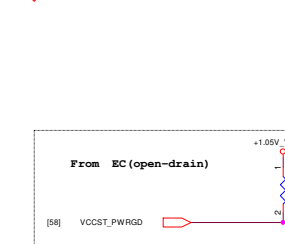
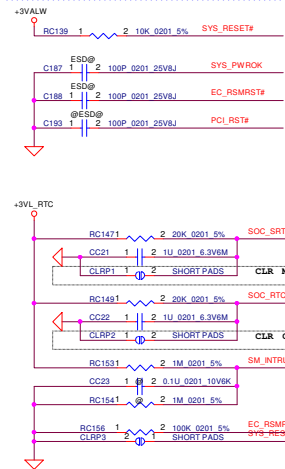
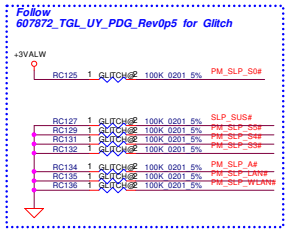


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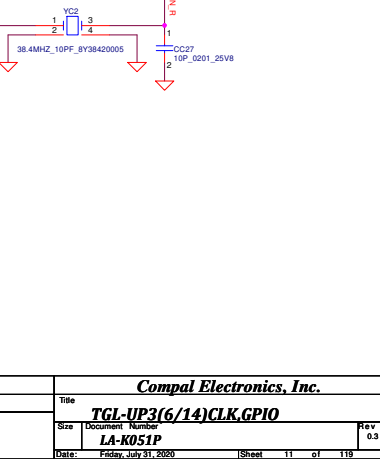
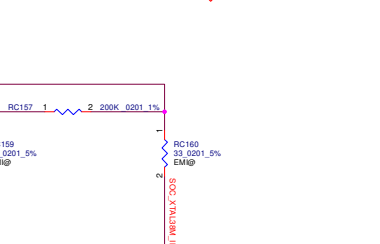
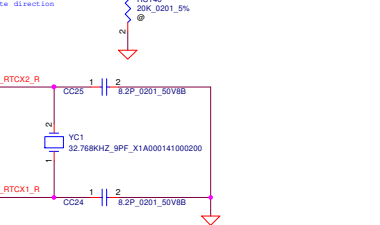
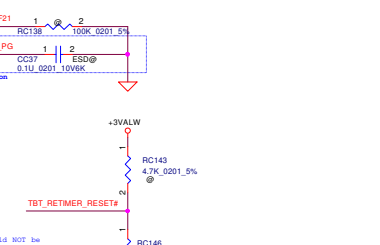
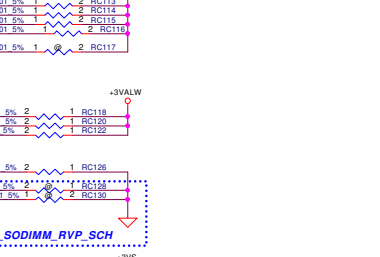
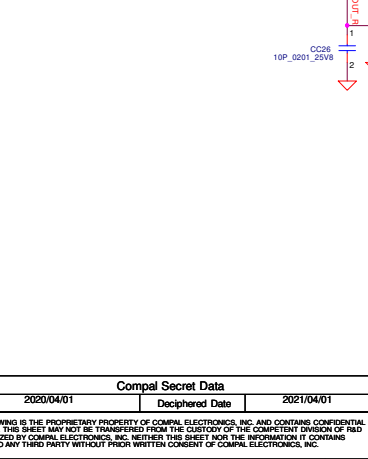
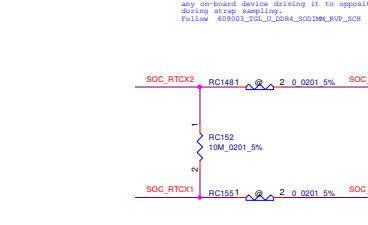
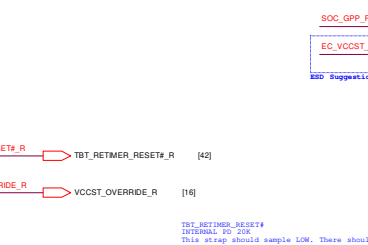
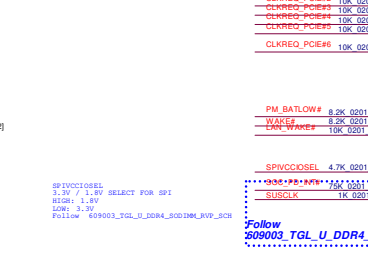
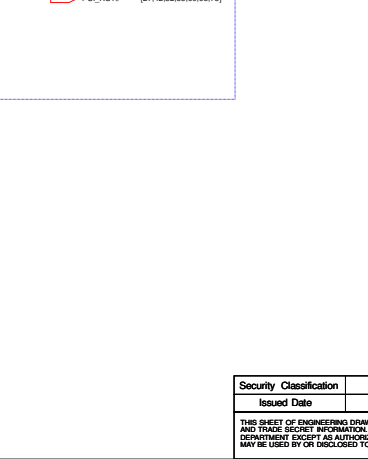
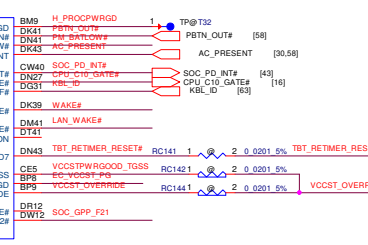
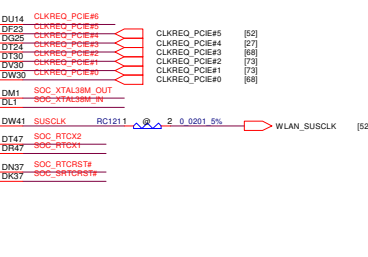
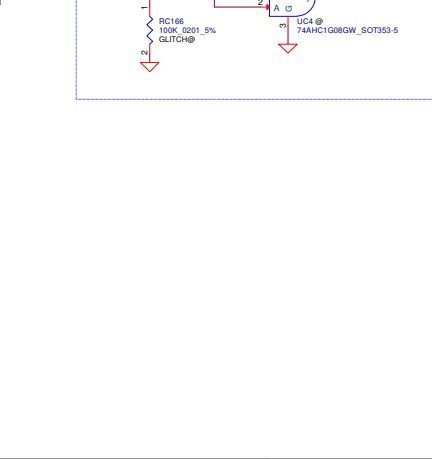
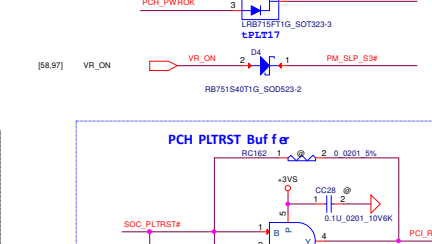
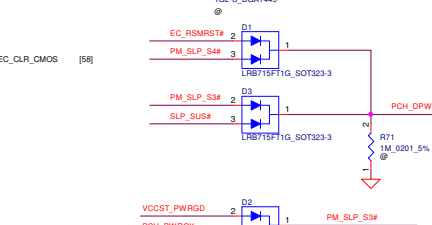
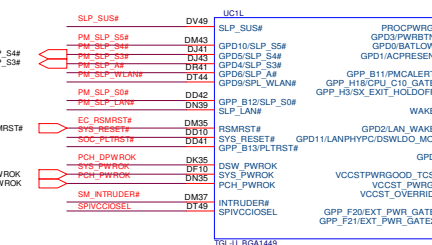
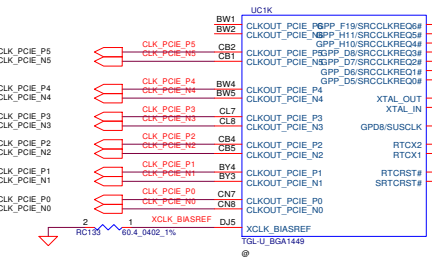


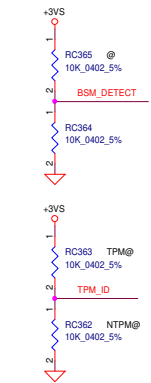
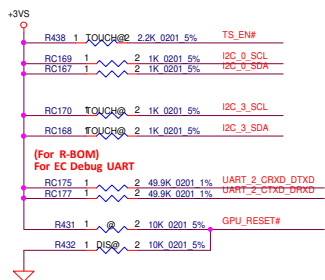
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PCIE CLK Gen4 only can use ch0,3,4



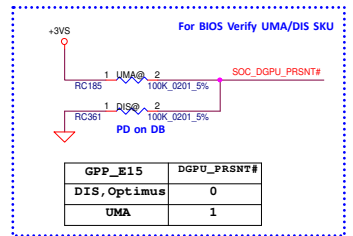
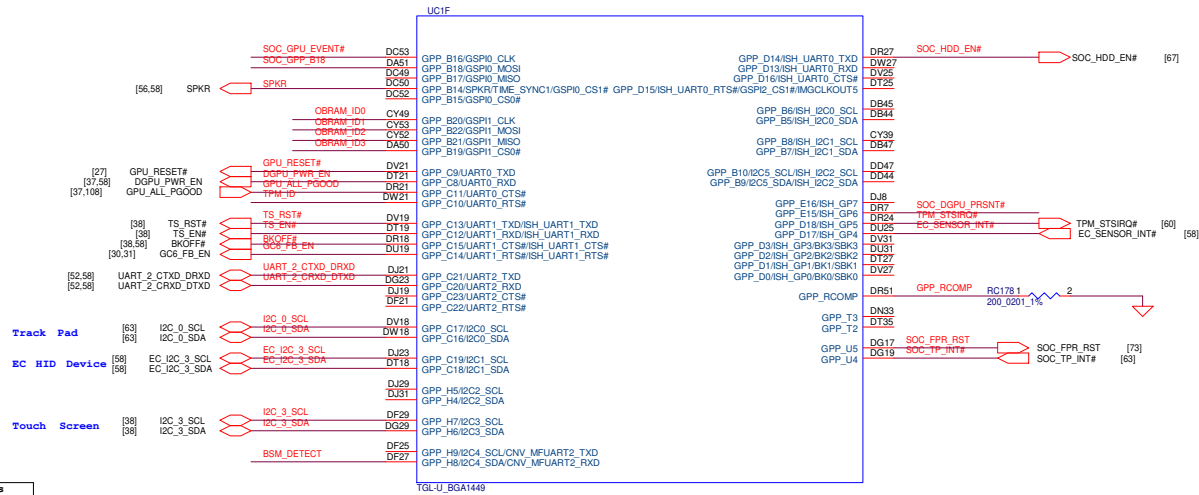
WLAN
dGPU
Second SSD2
Card Reader
LAN
Main SSD1



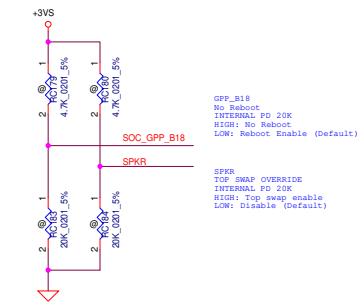


GPP_H8	Status
BattSaveMode Enable	0
BattSaveMode disable	1

GPP_C10	Status
TPM Stuff	1
TPM un-Suttf	0



Strap Pin



to dGPU Connect to SOC GPIO



place the same side(TOP/BOT) with on board RAM IC

Capacity	Description	OBRAM_ID3	OBRAM_ID1	OBRAM_ID0	BOM Structure
WITHOUT ON-BOARD RAM		L	L	L	NO_MD@
4GB	MT40A512M16TB-062E:J	L	L	H	DDR_M4G@
	HYNIX_H5AN8G6NCJR-XNC	L	H	L	DDR_H4G@
	SAMSUNG_K4A8G16SWC-BCWE	L	H	H	DDR_S4G@
8GB	MICRON_MT40A1G16RD-062E-E	L	H	L	DDR_M8G@
	H5ANAG6NCMR-XNC	L	H	H	DDR_H8G@
	Samsung_K4AAG16SWA-BCWE	L	H	L	DDR_S8G@

ON BOARD RAM

UD1 DDR_M4G@ MT40A512M16TB-062E:J SA0000CM500	UD2 DDR_M4G@ MT40A512M16TB-062E:J SA0000CM500	UD3 DDR_M4G@ MT40A512M16TB-062E:J SA0000CM500	UD4 DDR_M4G@ MT40A512M16TB-062E:J SA0000CM500
UD1 DDR_H4G@ H5AN8G6NCJR-XNC SA0000C2300	UD2 DDR_H4G@ H5AN8G6NCJR-XNC SA0000C2300	UD3 DDR_H4G@ H5AN8G6NCJR-XNC SA0000C2300	UD4 DDR_H4G@ H5AN8G6NCJR-XNC SA0000C2300
UD1 DDR_S4G@ K4A8G16SWC-BCWE SA0000C2500	UD2 DDR_S4G@ K4A8G16SWC-BCWE SA0000C2500	UD3 DDR_S4G@ K4A8G16SWC-BCWE SA0000C2500	UD4 DDR_S4G@ K4A8G16SWC-BCWE SA0000C2500
UD1 DDR_M8G@ MT40A1G16RD-062E-E SA0000D3U00	UD2 DDR_M8G@ MT40A1G16RD-062E-E SA0000D3U00	UD3 DDR_M8G@ MT40A1G16RD-062E-E SA0000D3U00	UD4 DDR_M8G@ MT40A1G16RD-062E-E SA0000D3U00
UD1 DDR_H8G@ H5ANAG6NCMR-XNC SA0000C2100	UD2 DDR_H8G@ H5ANAG6NCMR-XNC SA0000C2100	UD3 DDR_H8G@ H5ANAG6NCMR-XNC SA0000C2100	UD4 DDR_H8G@ H5ANAG6NCMR-XNC SA0000C2100
UD1 DDR_S8G@ K4AAG16SWA-BCWE SA0000C2200	UD2 DDR_S8G@ K4AAG16SWA-BCWE SA0000C2200	UD3 DDR_S8G@ K4AAG16SWA-BCWE SA0000C2200	UD4 DDR_S8G@ K4AAG16SWA-BCWE SA0000C2200

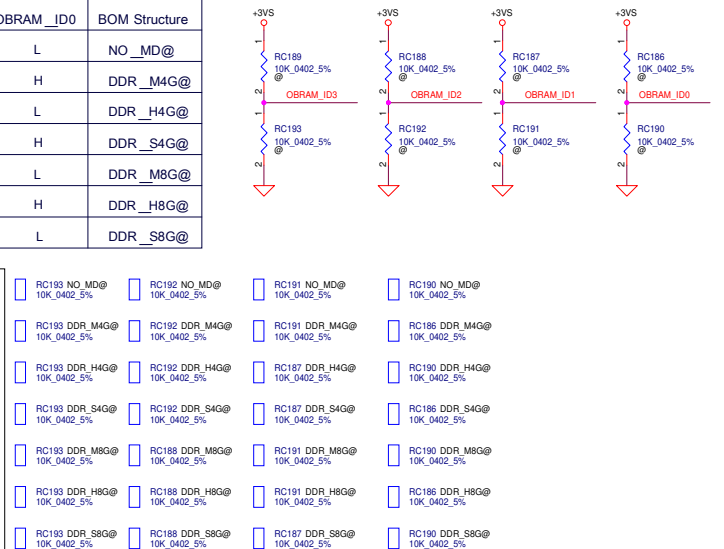
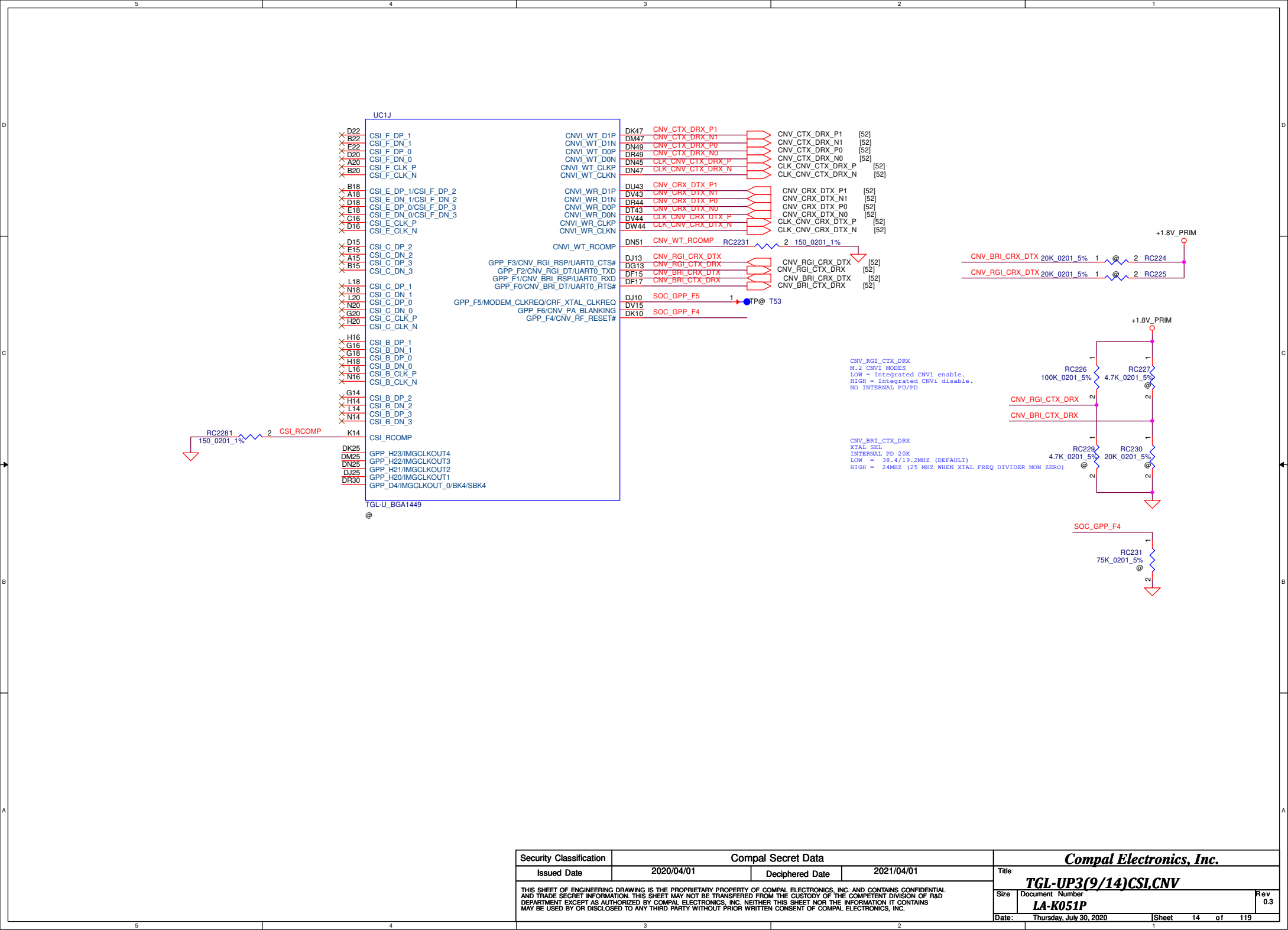


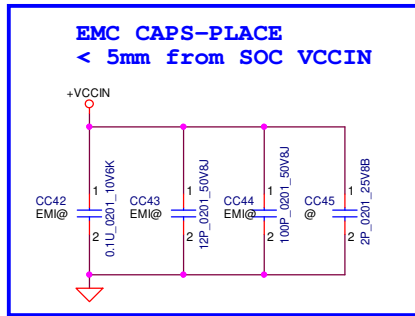
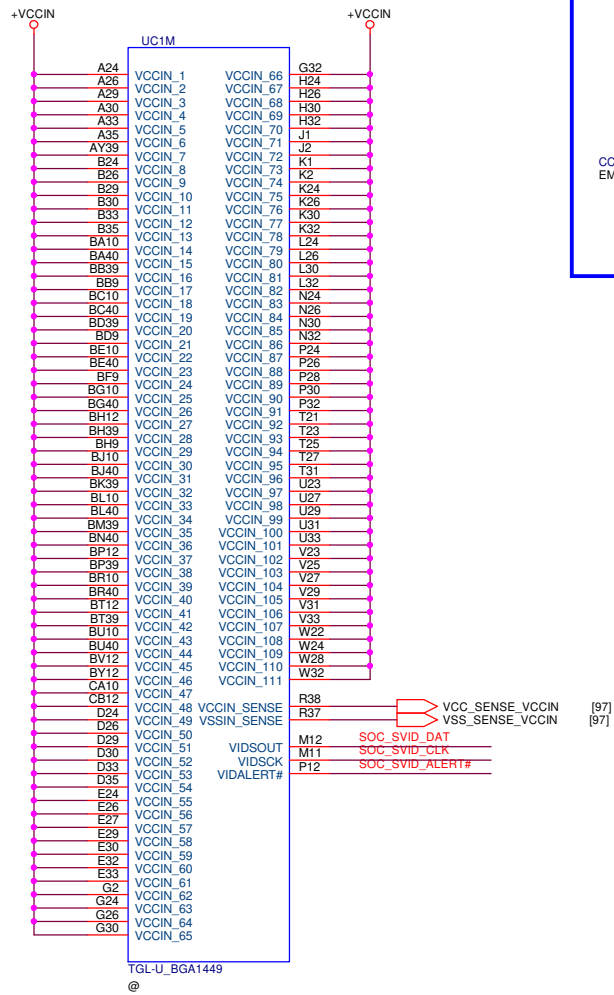


Table 58. Signal Descriptions

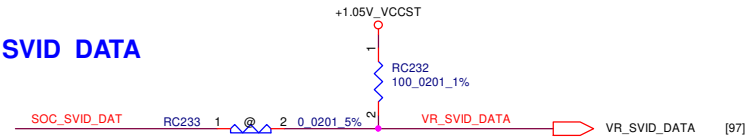
Name	Type	SSC Capable	Description
PCH-LP (U): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:0]CLKOUT_PCIE_N[6:0] PCH-LP (Y): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:1]CLKOUT_PCIE_N[6:1]	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices <ul style="list-style-type: none">CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 supportCLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support



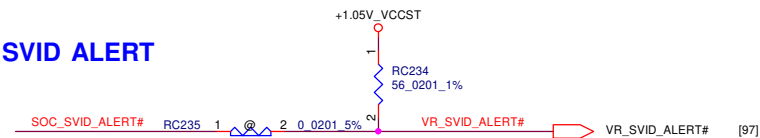
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							TGL-UP3(9/14)CSI,CNV					
							Size	Document Number				
							LA-K051P	0.3				
Date:							Thursday, July 30, 2020	Sheet 14 of 119				



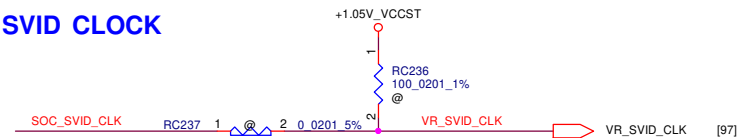
SVID DATA



SVID ALERT

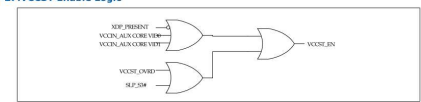
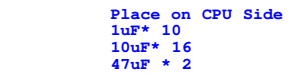


SVID CLOCK

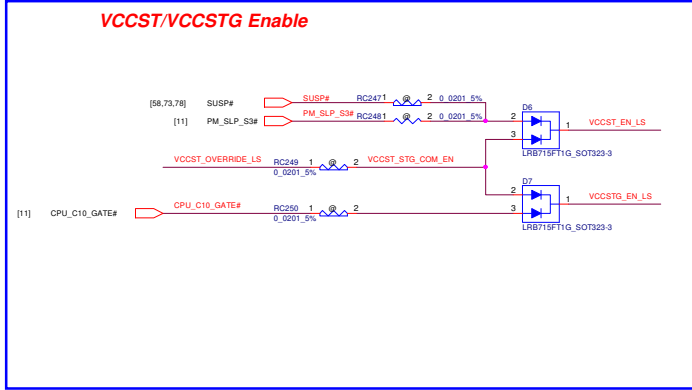


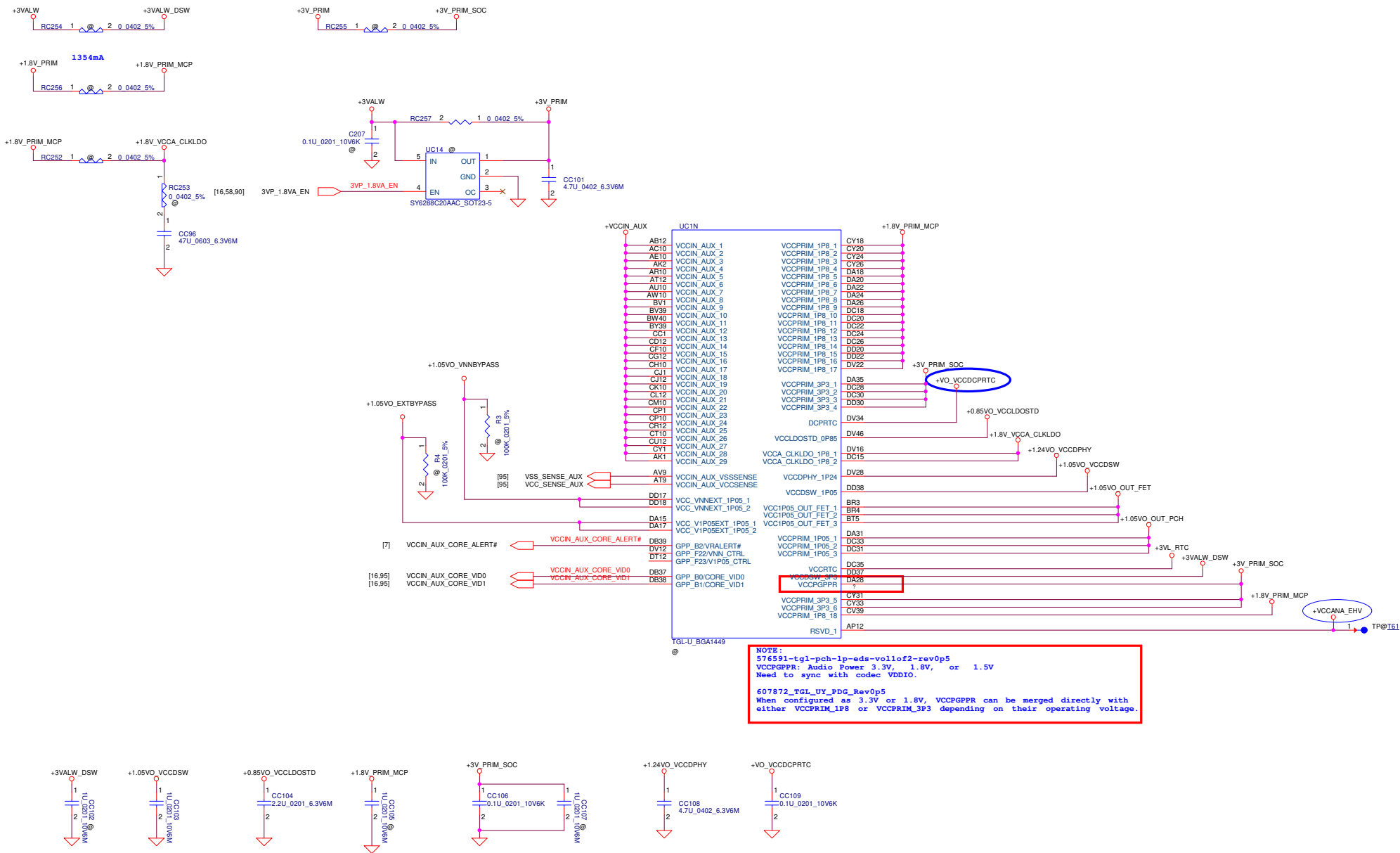
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Issued Date	2020/04/01	Deciphered Date	2021/04/01	Title		
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				Size	Document Number	Rev
				LA-K051P		
				Date: Thursday, July 30, 2020		
				Sheet 15 of 119		

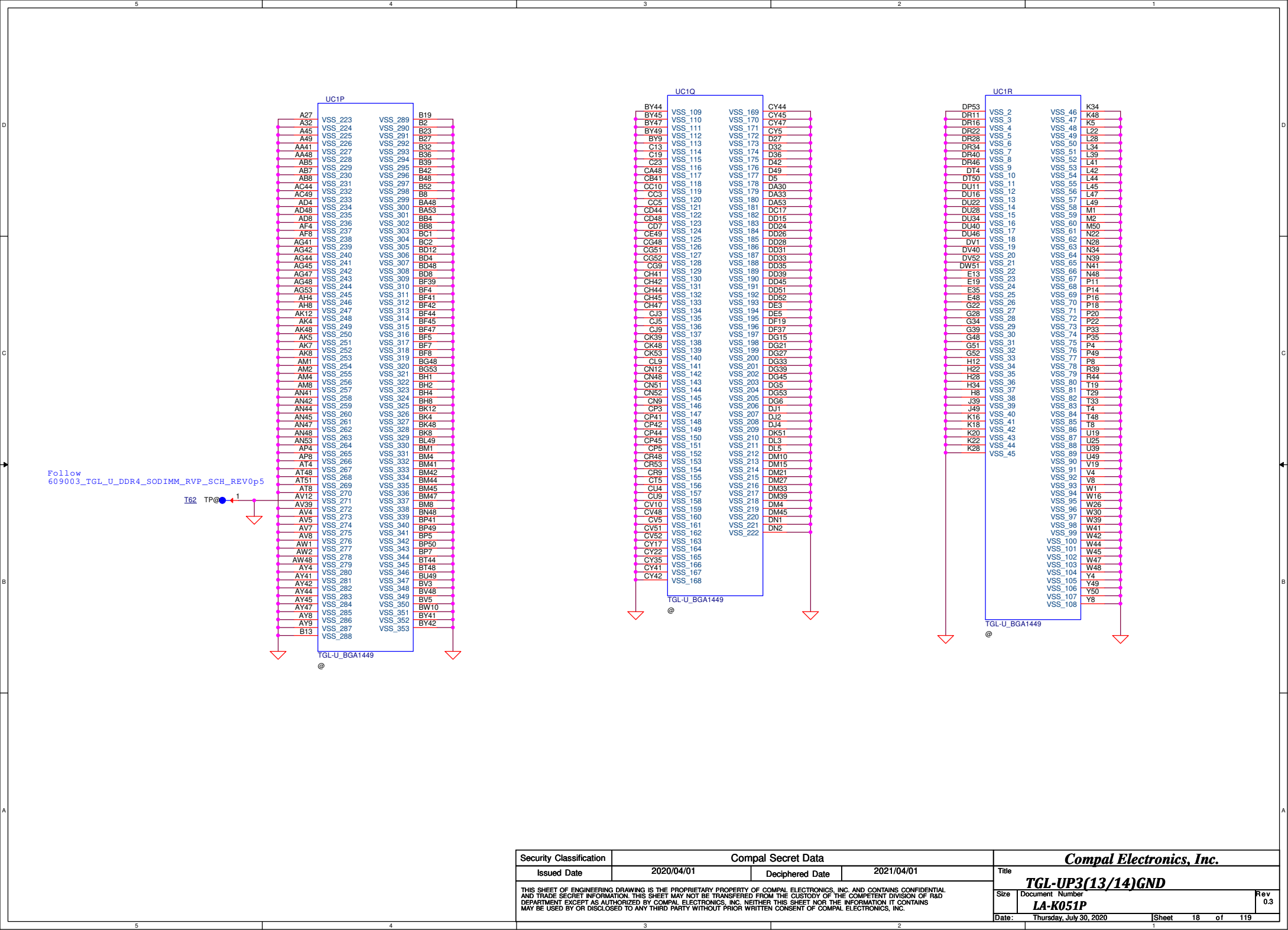
Three circuit diagrams are shown, each with a 1.2V source and a 1 ohm load resistor. The first diagram shows the inductor in series with the load. The second diagram shows the inductor in parallel with the load. The third diagram shows the inductor in series with the load, but with a 2P 0201 250AB capacitor in parallel with the inductor.

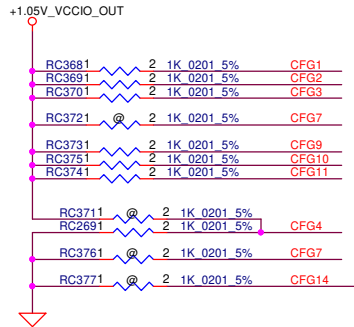


Singal Name		Input			
Premium	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_OVERRIDE_LS	D	H	D	L
	FM_SLP_S3# (SUSP#)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L
Volume	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_OVERRIDE_LS	D	H	D	L
	FM_SLP_S4# (SYS0N)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L







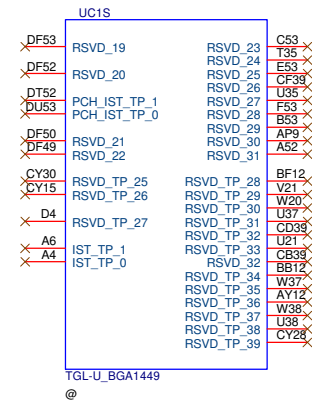
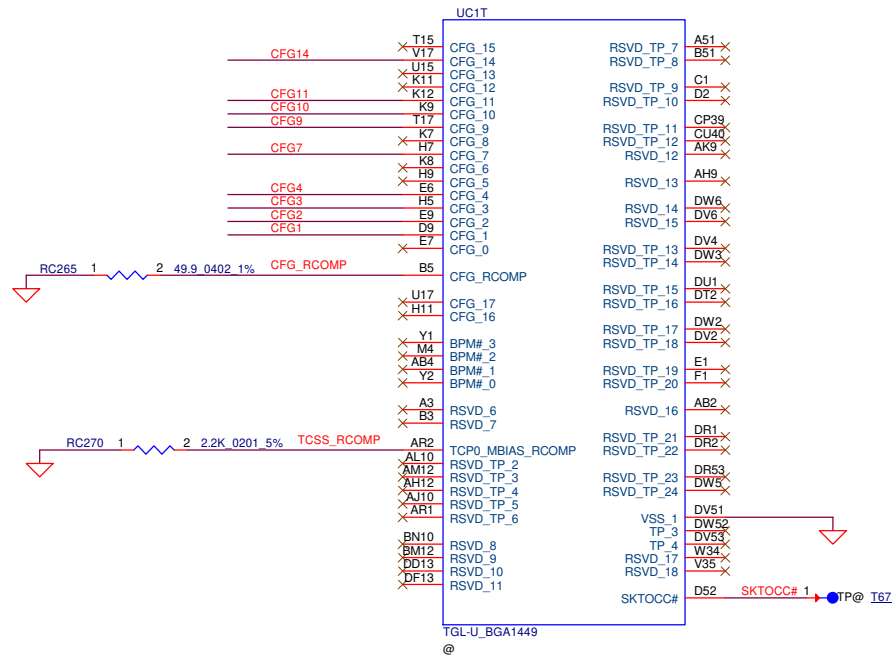


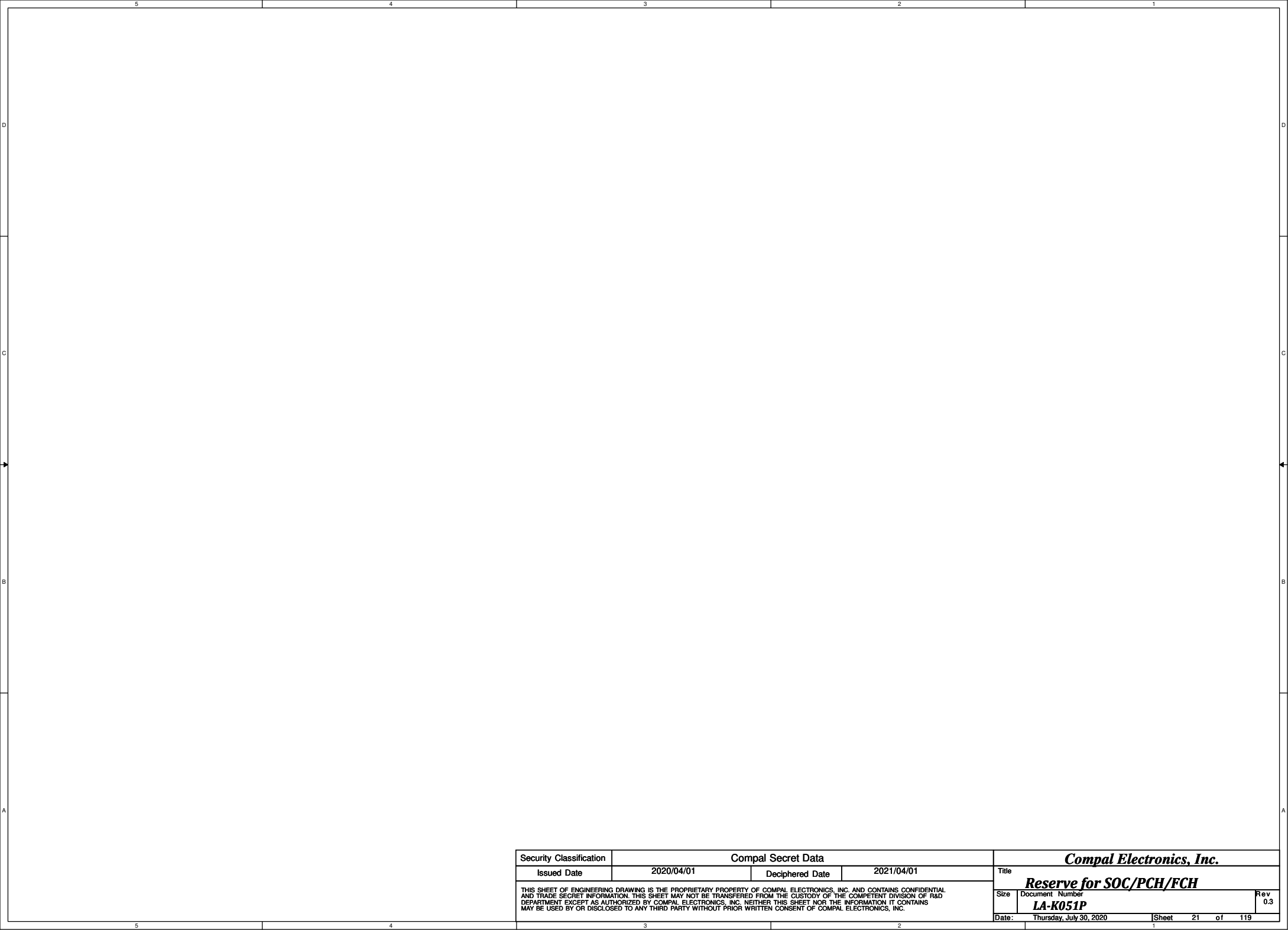
CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to
the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

CFG7
PEG Training
LOW : PEG Wait for BIOS for training.
HIGH : (default) PEG Train immediately following
RESET# de assertion.

CFG14
PEG60 Lane Reversal
HIGH : (Default) Normal
LOW : Reversed

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull- down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull- down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull- down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

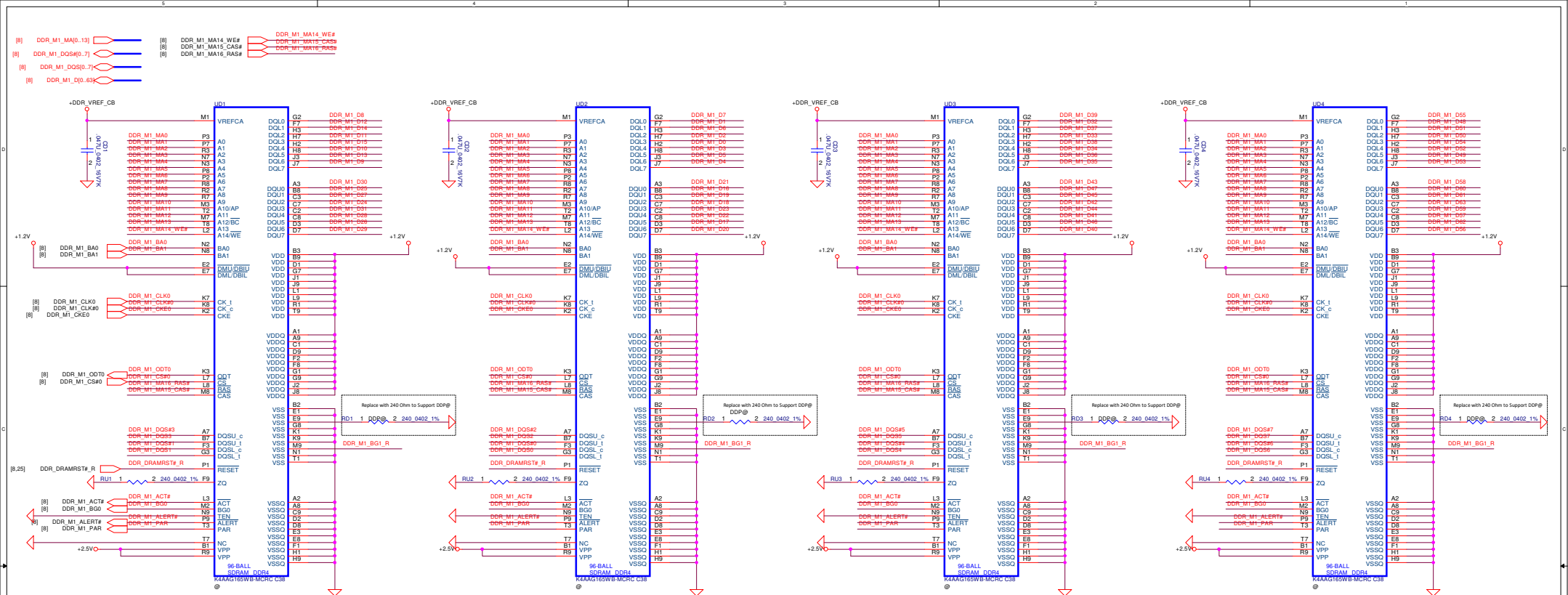




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				Size	Document Number	Rev
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Date:		Thursday, July 30, 2020		Sheet	21 of 119	

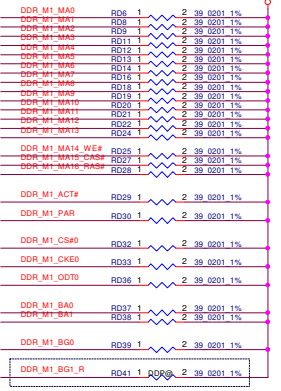
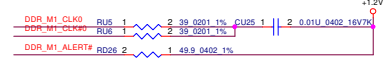
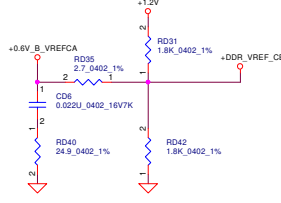
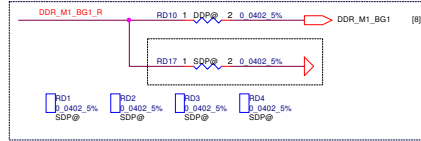


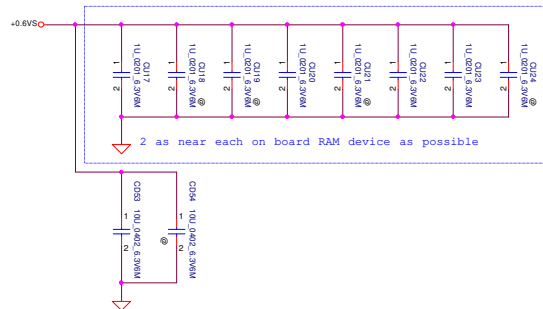
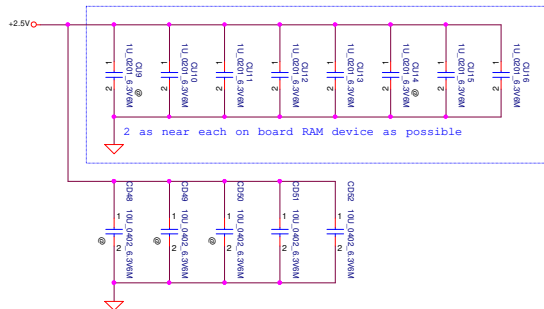
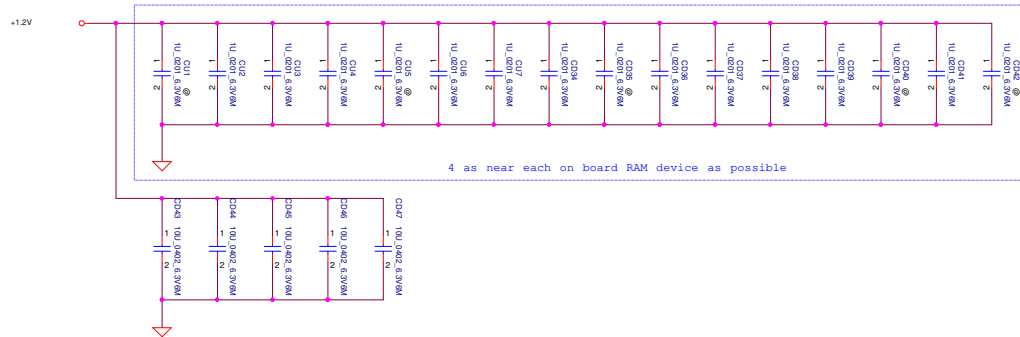
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					Size	Document Number	Rev
					LA-K051P		0.3
					Date:	Thursday, July 30, 2020	Sheet 22 of 119

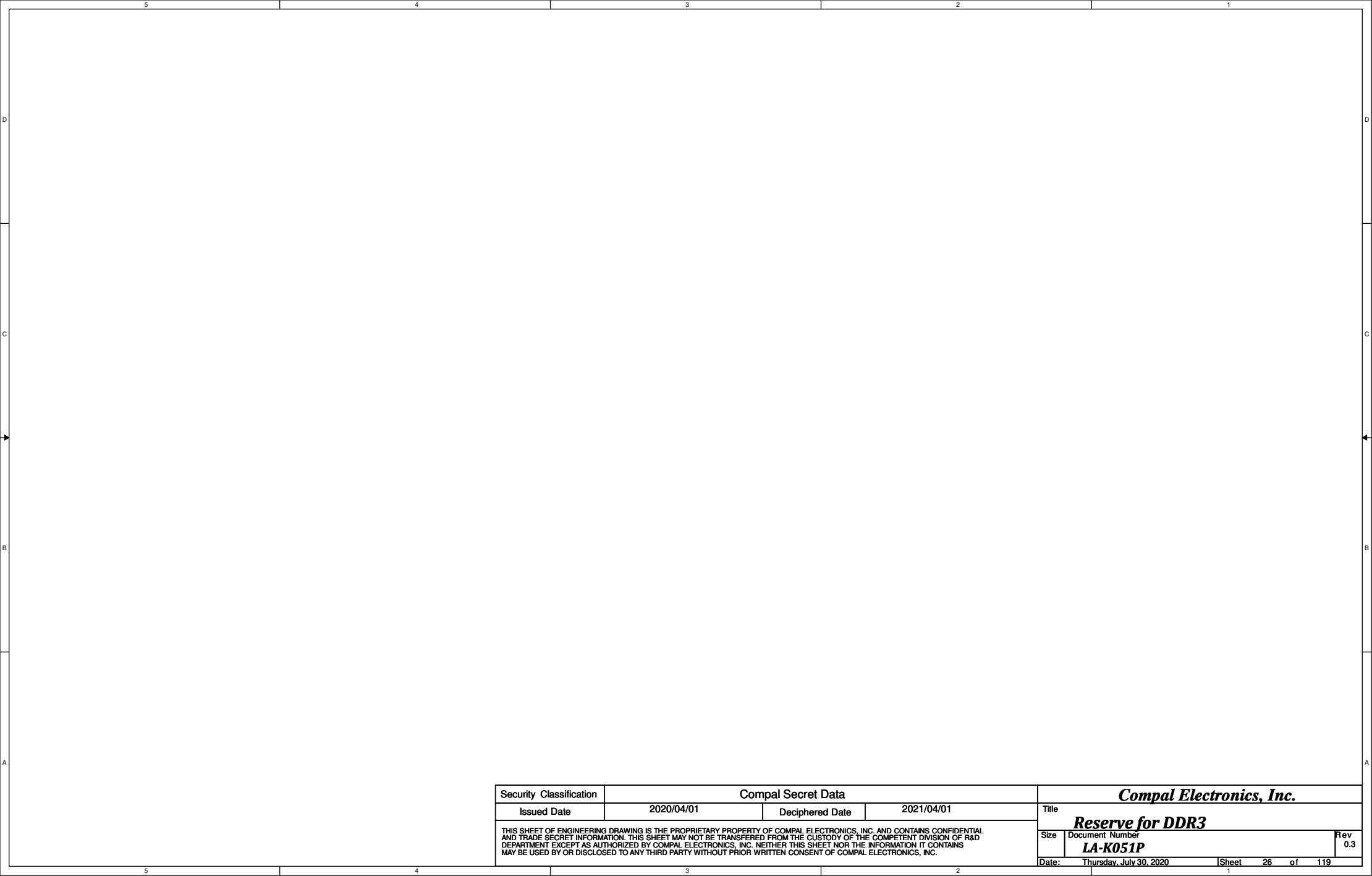


CLOCK TERMINATION

Co-lay for SDP / DDP Memory DIE





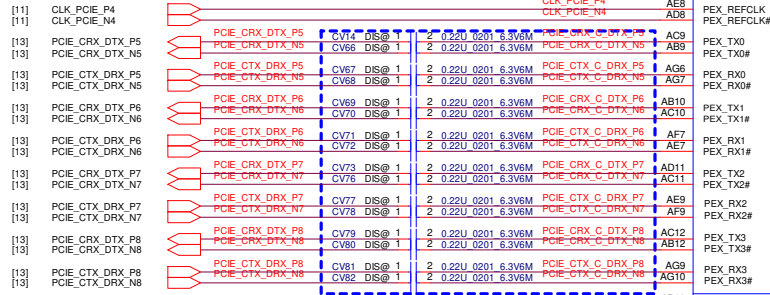


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				Size	Document Number
					LA-K051P
Date:		Thursday, July 30, 2020		Sheet	26 of 119
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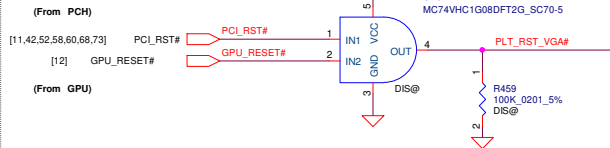
GPU

PCIE CLK

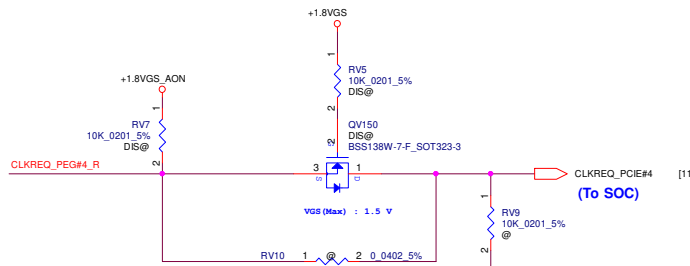
PCIE X4 Bus



Reset Control



CLK_REQ



U1A

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

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N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

PEX LINES 15 - 4 ARE DEFEATED

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

N18S-G5-FCBGA603

PEX_CVDD

PEX_HVDD

PEX_PLL_HVDD

PEX_PLL_HVDD

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

PEX_TERM

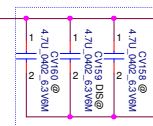
PEX_TERM

PEX_TERM

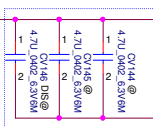
PEX_TERM

PEX_TERM

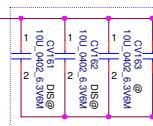
Place under GPU



Place under GPU



Place near BGA



Place near BGA

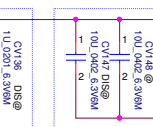
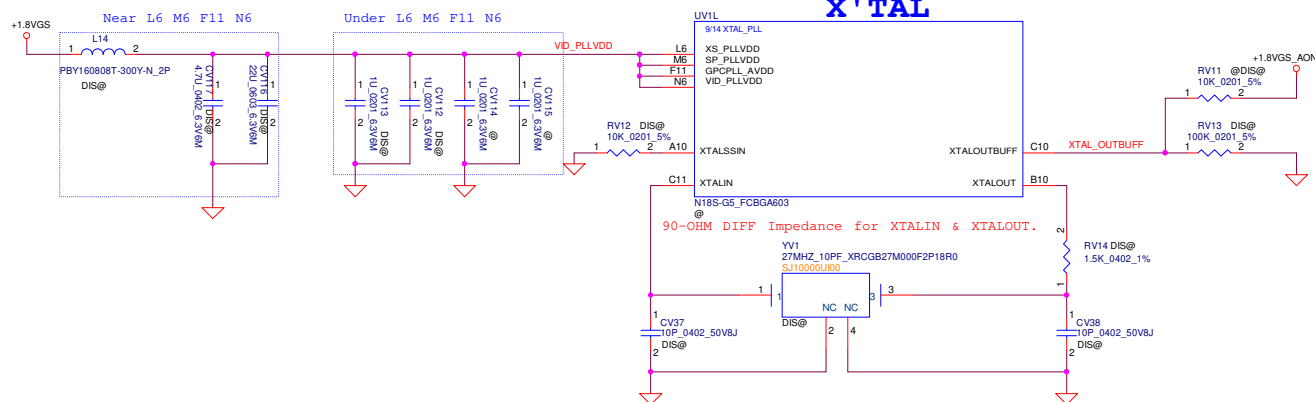
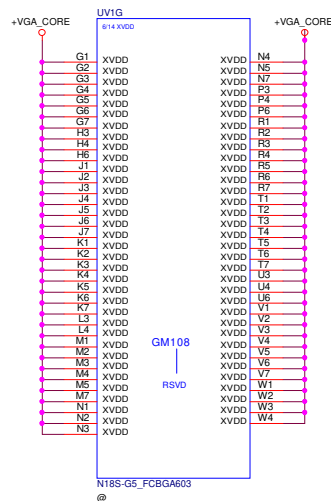
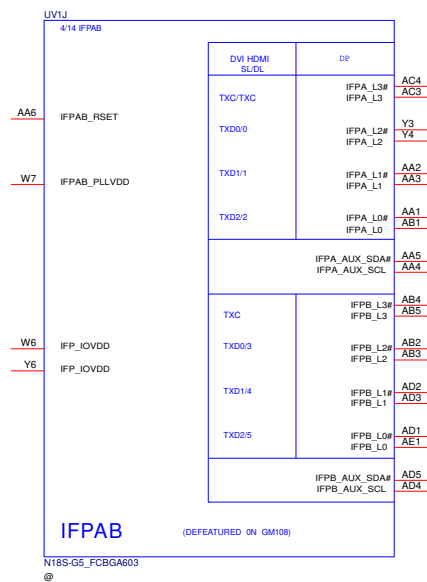
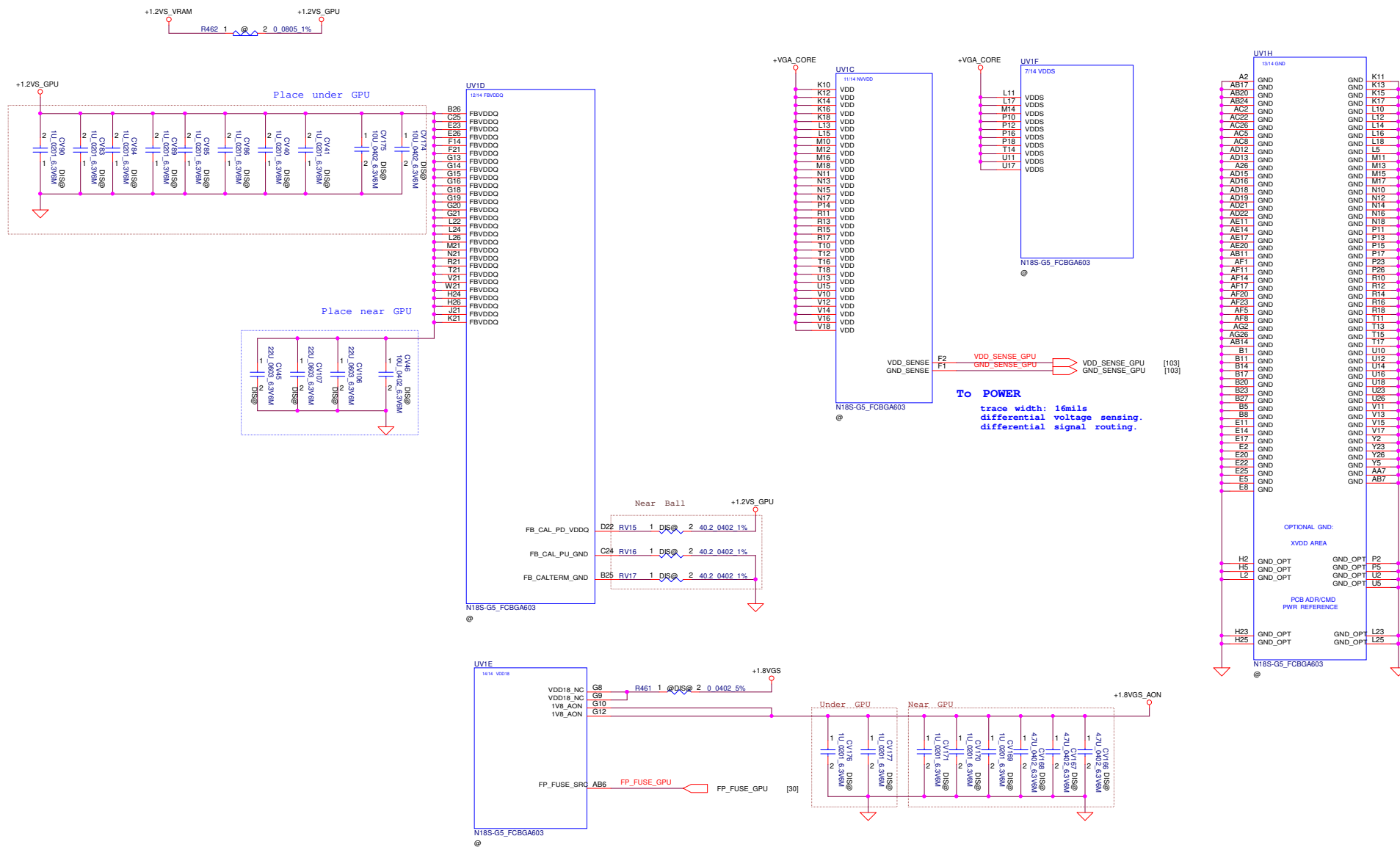
SA0000DGW00
SIC N18S-G5-A1 BGA 603P ES S

Table 3-17. PEX_PLLVDD Decoupling

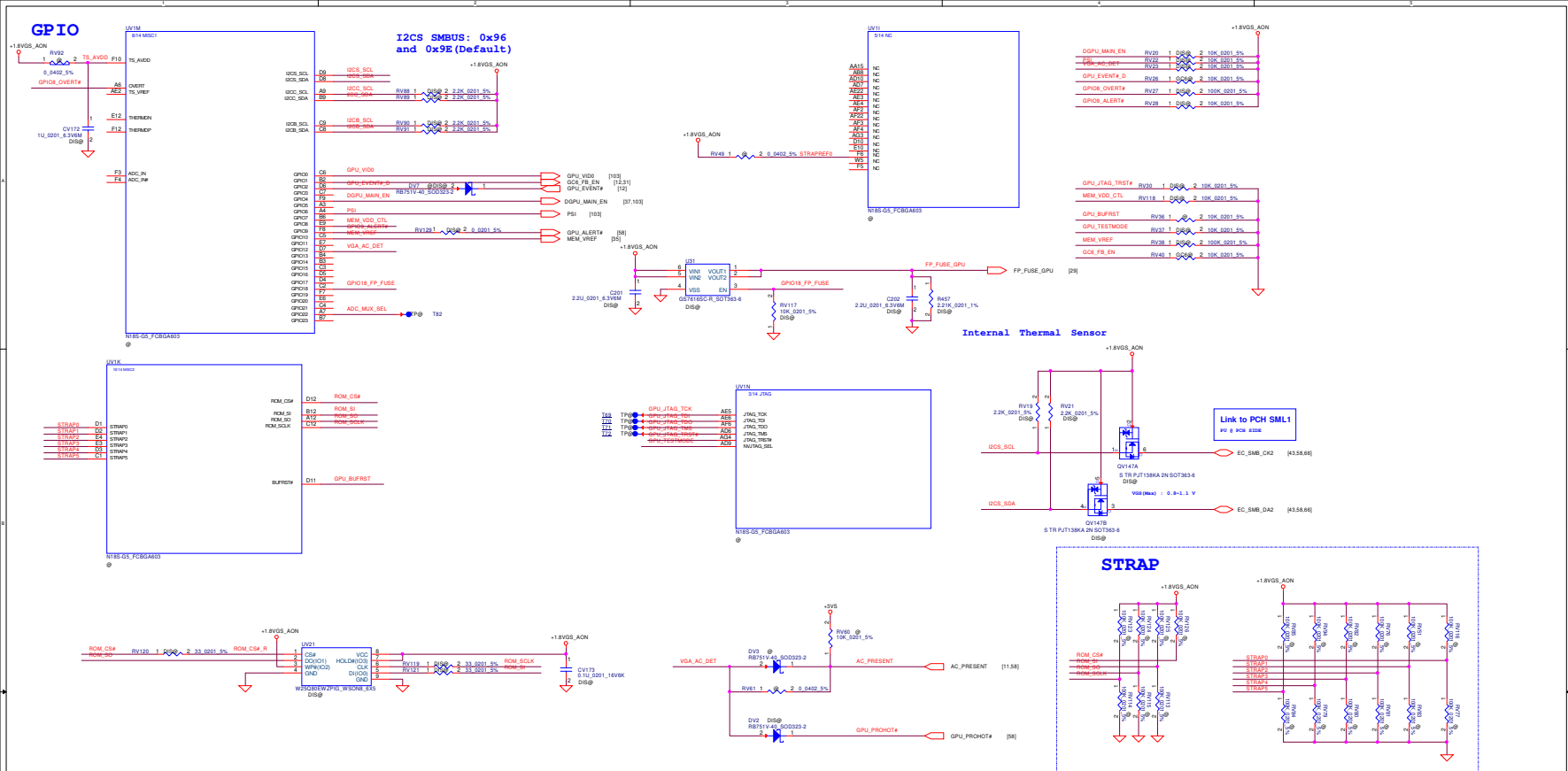
Capacitor Type	Footprint	Population	Location
0.1 μ F	X7R	0402	1 Under GPU
1.0 μ F	X5R	0603	1 Near GPU
4.7 μ F	X5R	0805	1 Near GPU





** XPWR pins are configurable.
 These pins are not connected on the substrate.
 Therefore, XPWR pins can be assigned as needed,
 to improve Top layer routing, power delivery.

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						Size		Document Number		Rev	
						LA-K051P				0.3	
						Date:		Thursday, July 30, 2020		Sheet 29 of 119	



N18S-G5 VRAM Strap										
RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE						
0x1 MT61K25M32J-14:A	RV101 DIS@ 100K, 0.001, 5%	RV103 DIS@ 100K, 0.001, 5%	RV118 VRAM, MS@P 100K, 0.001, 5%							
0x0 K4280325BC-HC14			RV117 VRAM, MS@P 100K, 0.001, 5%							

DDR6 RAM_CFG										
GPU	Memory Type	FBVDD/FBVDDQ	Memory Density	Memory configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CLK	Memory D/C Minimum	Status
N18S-G5	DDR6	1.20V	8Gb	2chx256Mb16	Micron	MT61K25M32E-14A	A-die	14 Gbps	1940	Production Candidate
					Samsung	K4280325BC-HC14	C-die	14 Gbps	2001	Production Candidate

N18S Strap					
Item	N18S-G5				MS-Hybrid Mode
Device ID	Primary: Secondary: N/A				
Package	GB2E-64				
Internal P/N					
ROM_SCLK (LSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
ROM_SI	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
ROM_SO (MSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
Strap0 (LSB)	Refer to N18s_RAM_Straps table				
Strap1					
Strap2 (MSB)					
Strap3 (LSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
Strap4	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
Strap5 (MSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PU to GND				L
Boot Voltage	0.8V				



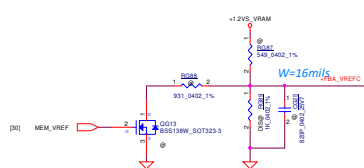
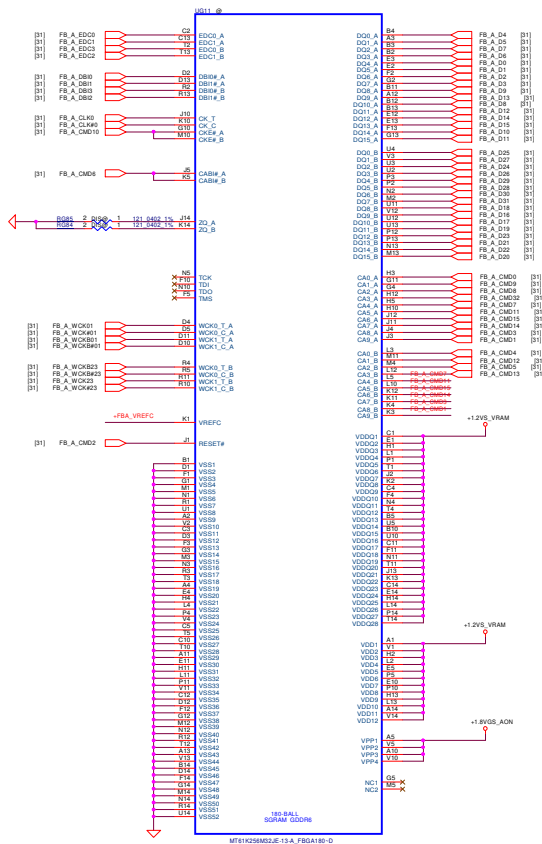
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				Date:	Thursday, July 30, 2020	0.3
				Sheet	33	of 119



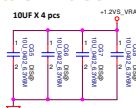
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								Size		Document Number		Rev	
								LA-K051P		0.3			
								Date:		Thursday, July 30, 2020		Sheet 34 of 119	

VRAM A

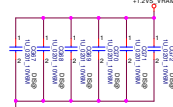
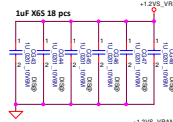
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GM_A	GM001	GM000
GM_A	GM002	GM001
GM_A	GM003	GM002
GM_A	GM004	GM003
GM_A	GM005	GM004
GM_A	GM006	GM005
GM_A	GM007	GM006
GM_A	GM008	GM007
GM_A	GM009	GM008
GM_A	GM010	GM009
GM_B	ChapBook 6.5	ChapBook 6.7
GM_B	GM011	GM010
GM_B	GM012	GM011
GM_B	GM013	GM012
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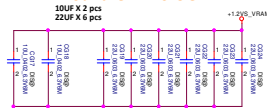
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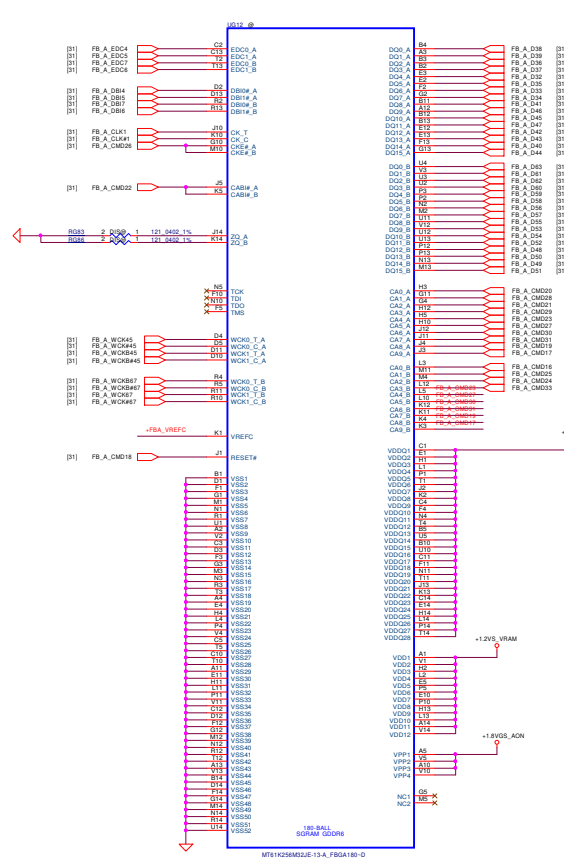
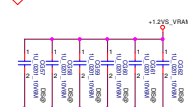
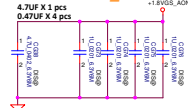
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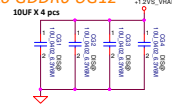
Around GDDR6 UG11



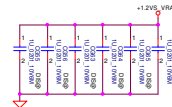
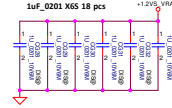
Close to +1.8VGS_AON



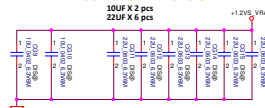
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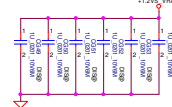
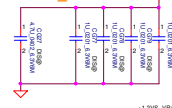
Close to GDDR6 UG1



Around GDDR6 UG12



Close to +1.8VGS_AOM

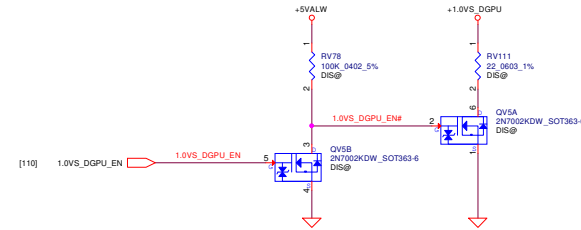
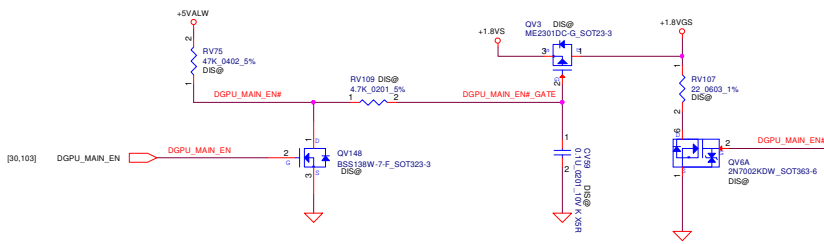


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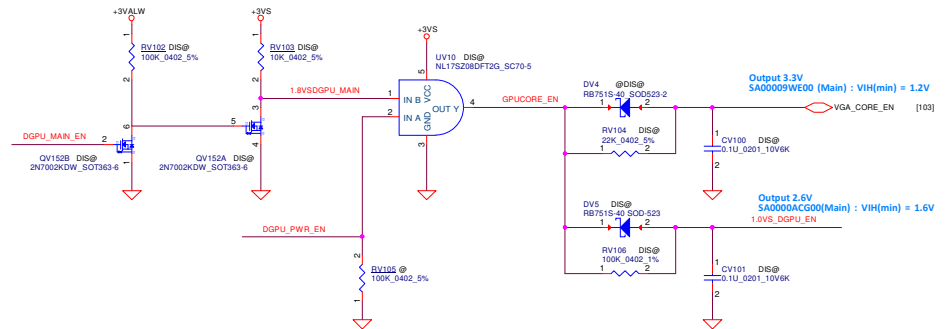
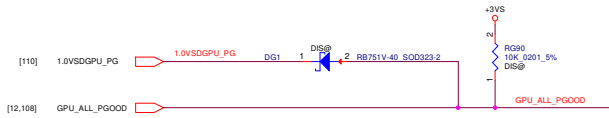
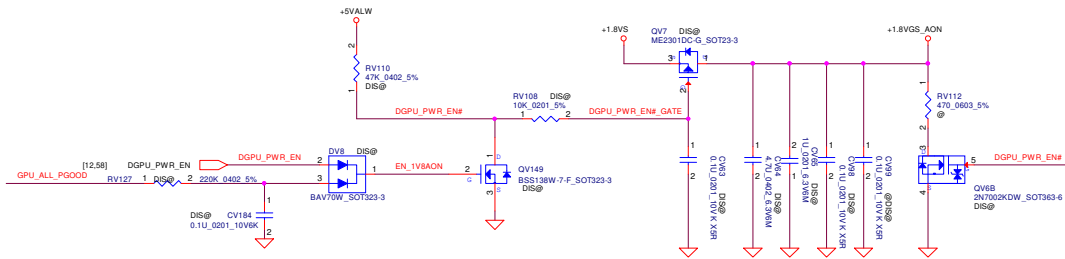


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								Date:		Thursday, July 30, 2020		Sheet 36 of 119	

+1.8VS to +1.8VGS



+1.8VS to +1.8VGS_AON



7.3.2.1 Power-Up Sequence

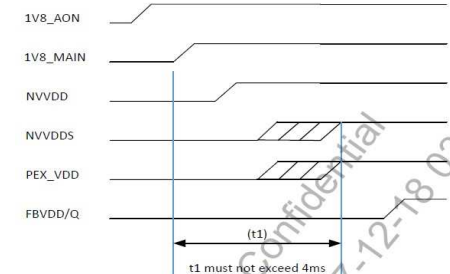
The following power-up sequence is required:

1V8_AON → 1V8_MAIN → NVVDD → NVVDDS / PEX_DVDD → FBVDD(Q)

► All GPU power rails must ramp up after 1V8_AON.

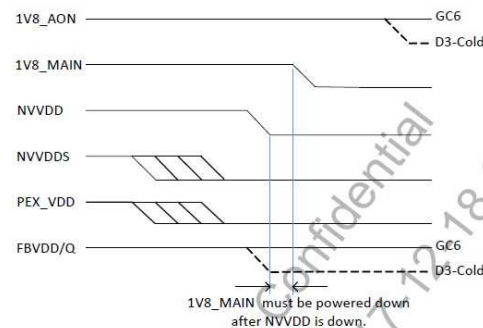
► FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.



re 7.5 Example of Power-Up Sequencing Order

7.3.2.2 Power-Down Sequence



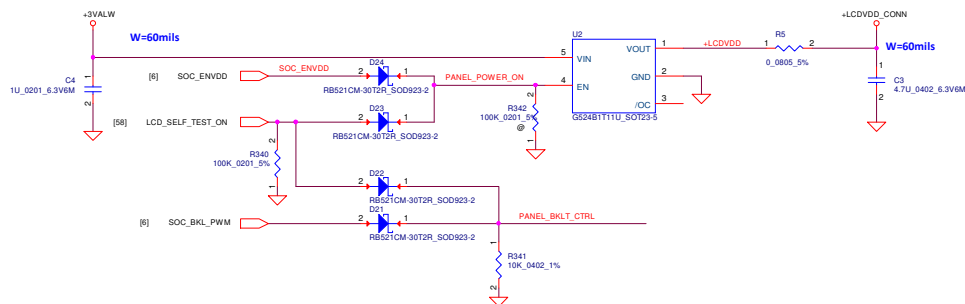
1V8_MAIN must be powered down after NVVDD is down.

Figure 8.9 GC OFF Entry/Exit Timing Diagram

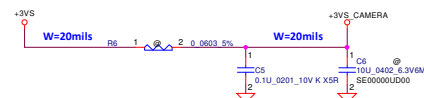
Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

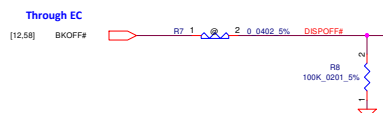
LCD POWER SWITCH



CAMERA POWER CIRCUIT



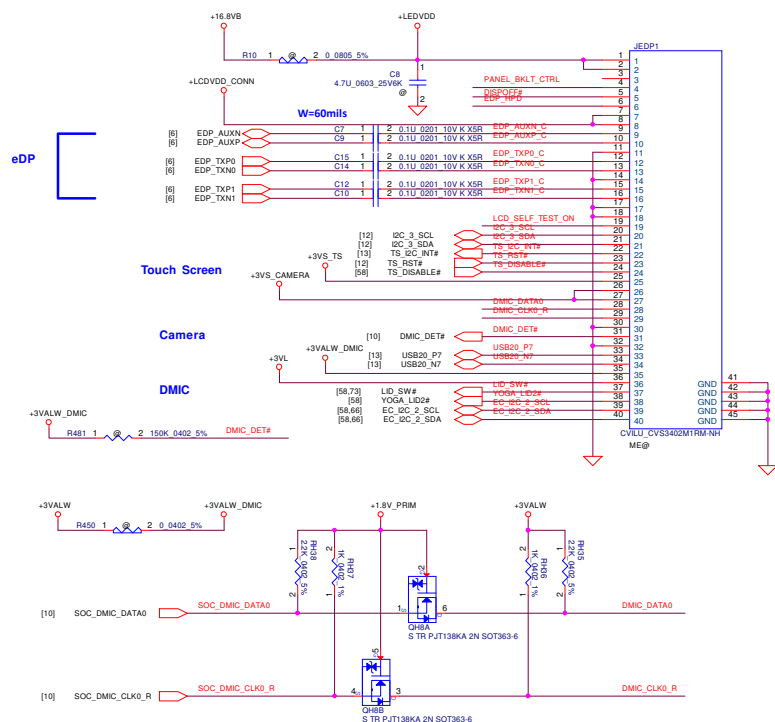
DISPLAY OFF



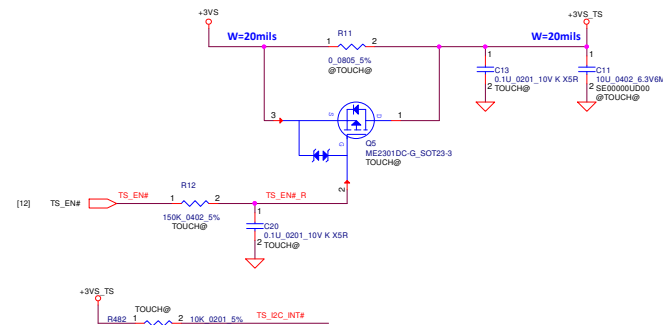
HOT PLUG DETECT



eDP CONNECTOR

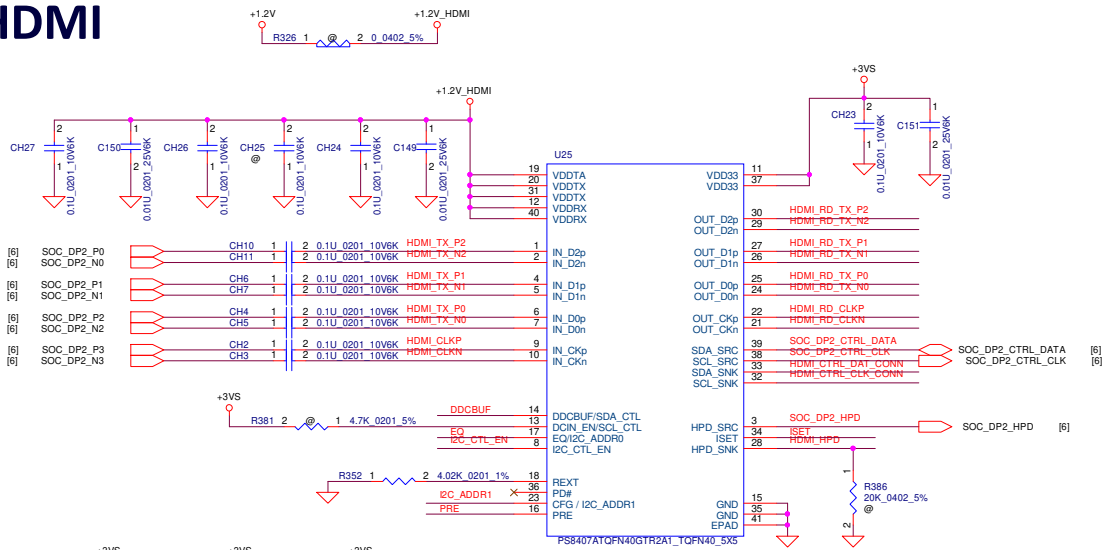


Touch Screen POWER CIRCUIT



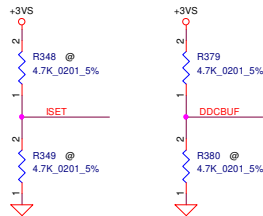
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HDMI



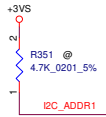
Output pre-emphasis setting; Internal pull down at ~150kohm, 3.3V I/O.

L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis



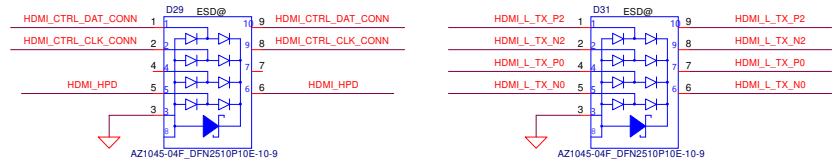
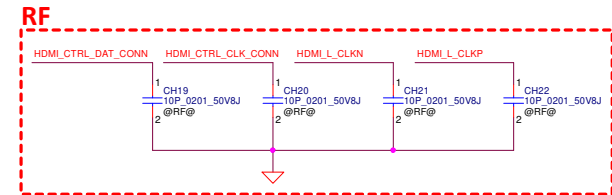
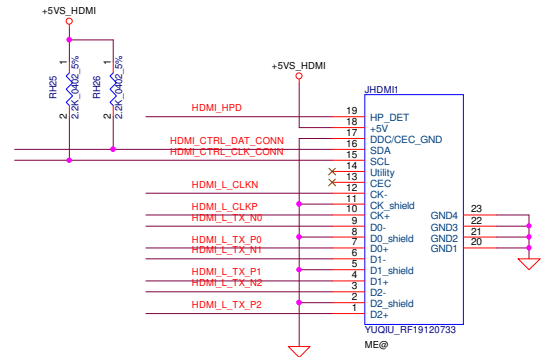
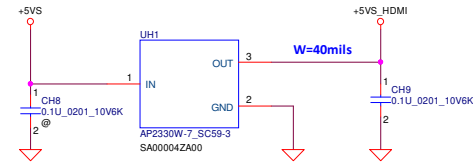
TMDS output swing adjustment; Internal pull down at ~150kohm, 3.3V I/O.

L: default
H: increase +13%
M: reduce -13%



I2C control bus address LSB; Internal pull down at ~150kohm, 3.3V I/O.
[I2C_ADDR1, I2C_ADDR0]=

LL: 0x4C/4D (default)
LH: 0x5C/5D
HL: 0xCC/CD
HH: 0xEC/ED



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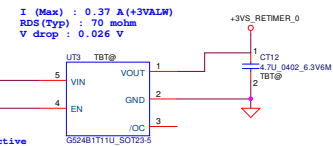
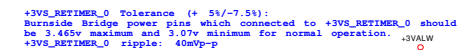
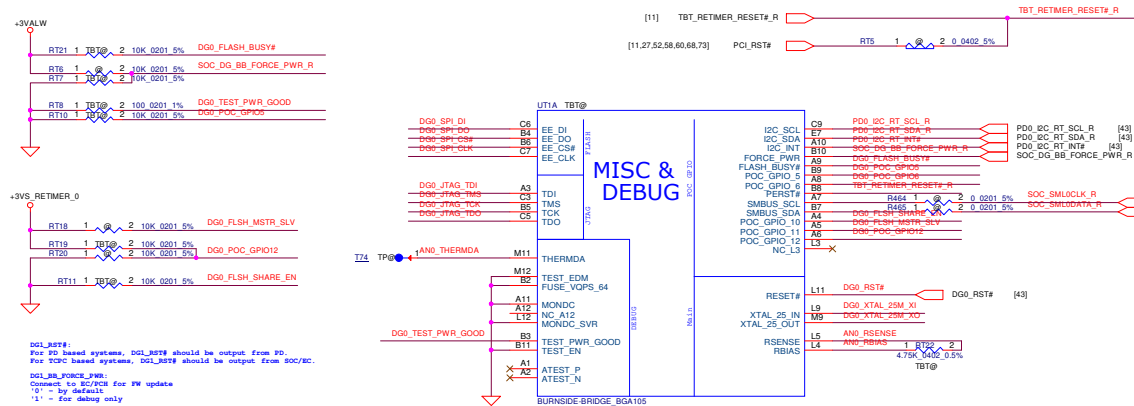


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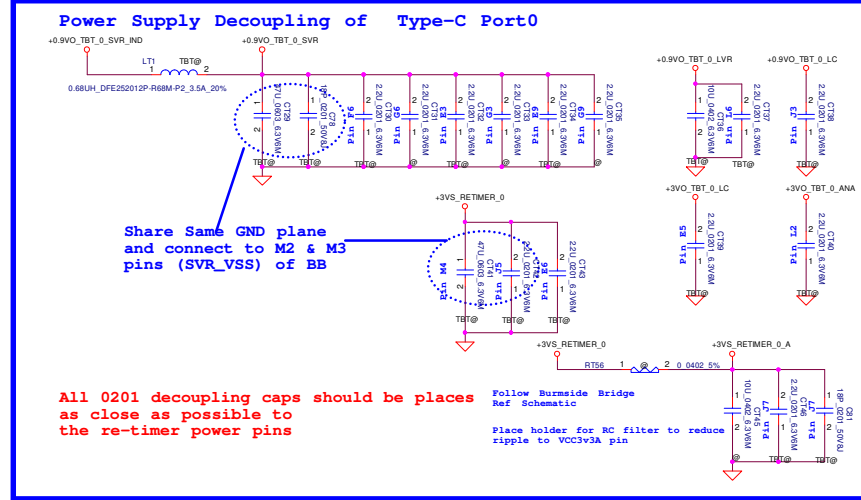
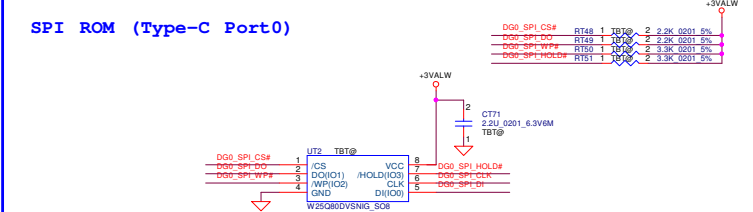
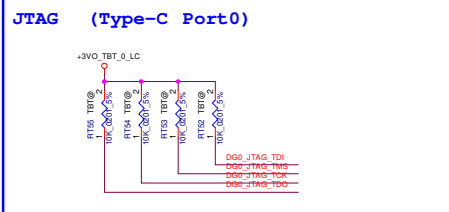
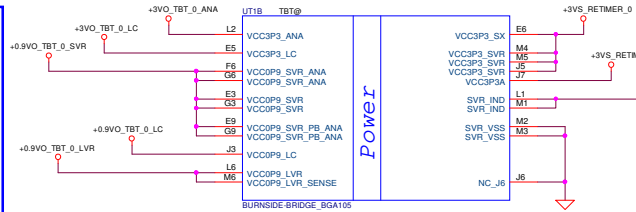
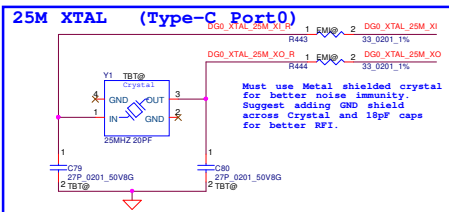
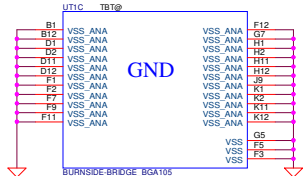
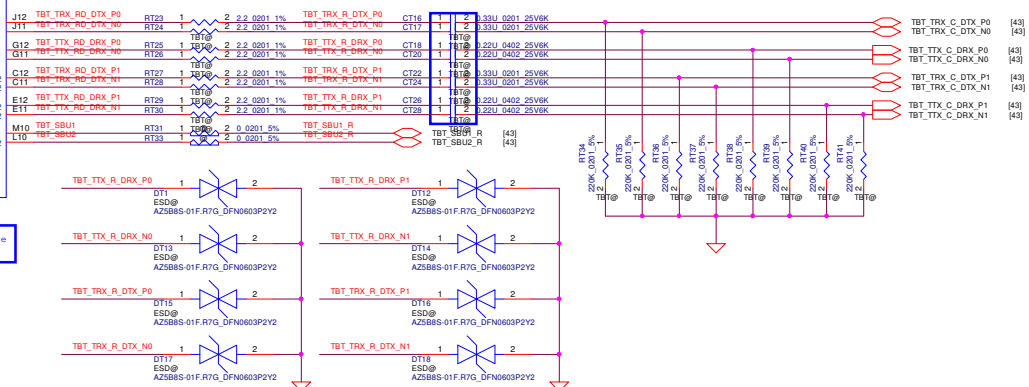
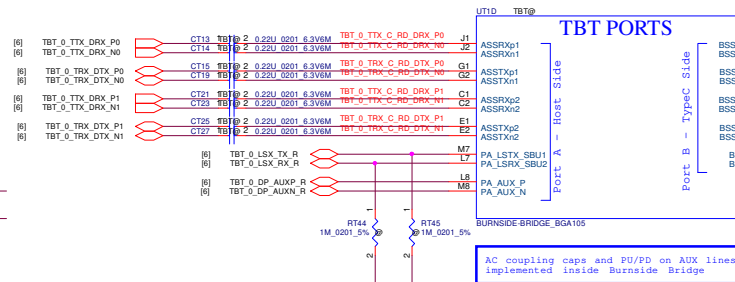
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				Size	Document Number	Rev
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MB USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)

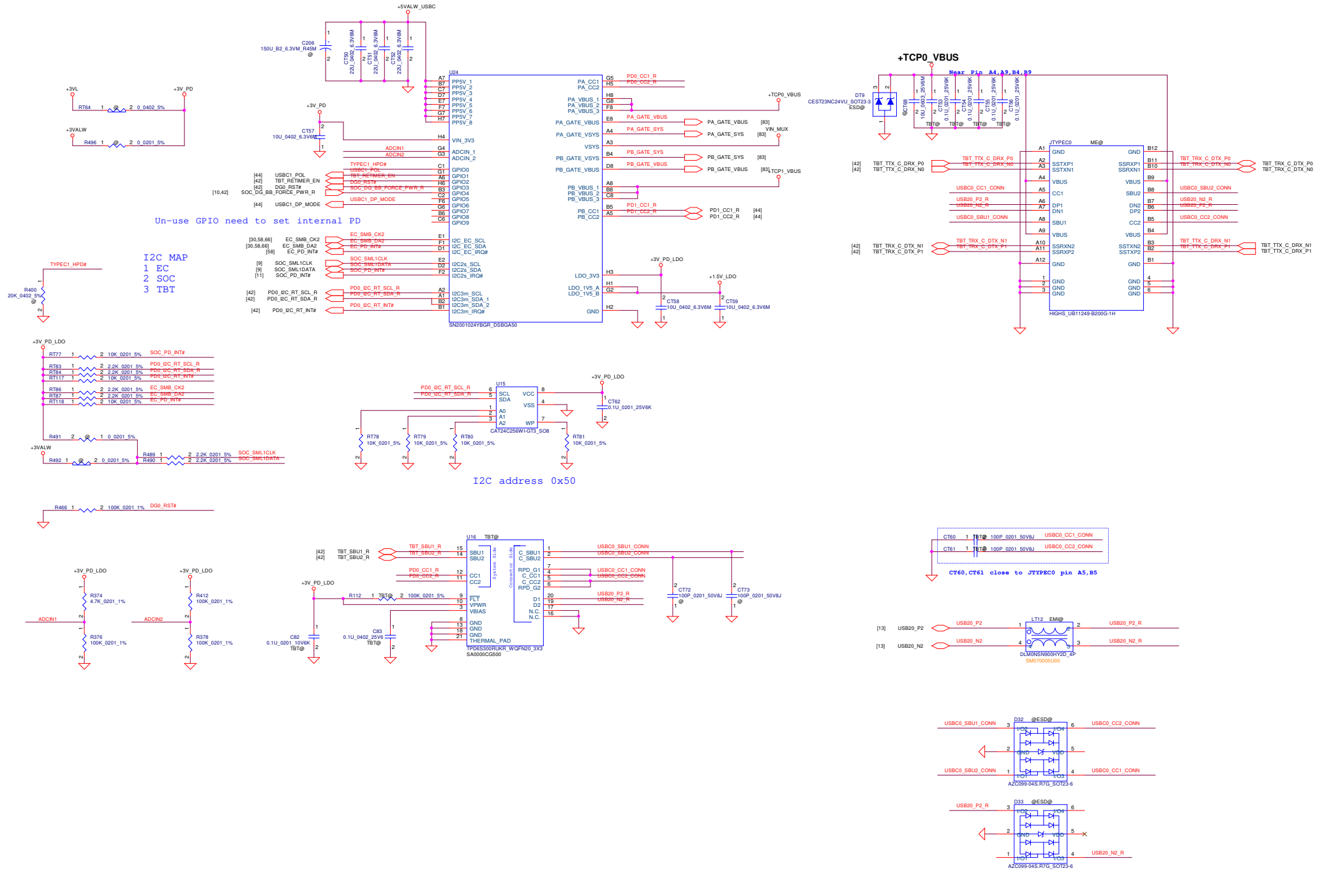


NOTE:
Re-Timer with TBT , AC Caps should be use 0201/25V package.
Re-Timer without TBT , AC Caps can be use 0402/25V package.
For non-PD support 25V rating is no must.

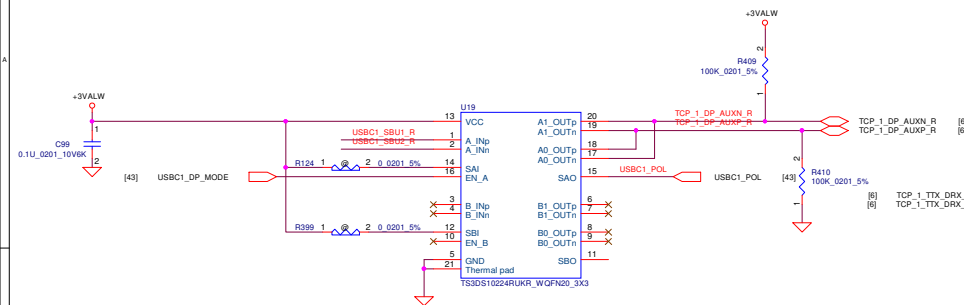
Due to material shortage,ORB use 0402 instead of 0201 package.



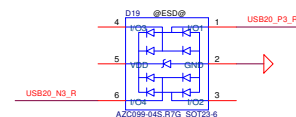
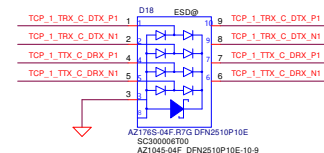
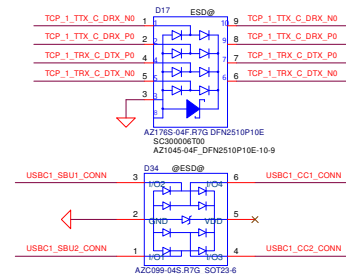
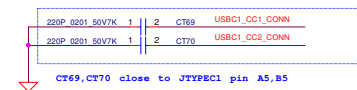
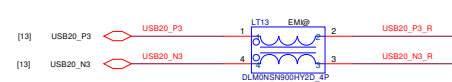
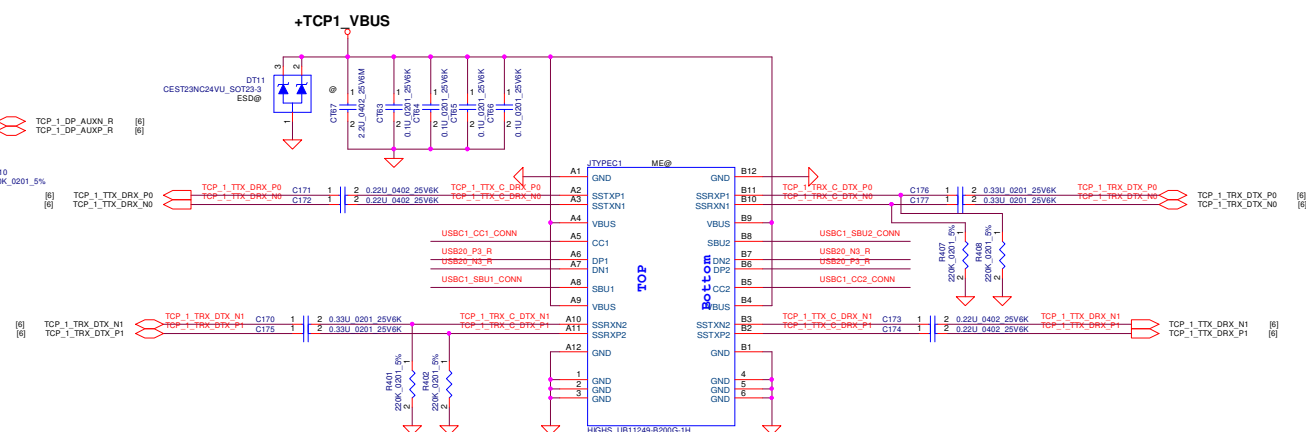
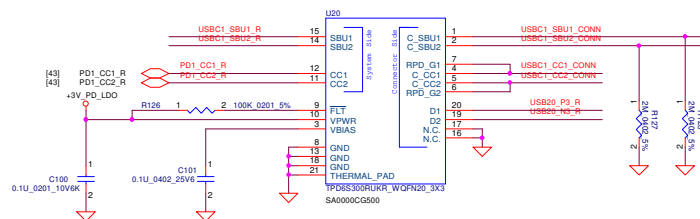
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Type-C PORT 1



SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
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0001	INB	—	—	INA
0010	INB	—	INB	—
0011	INB	—	—	INB
0100	—	INB	INA	—
0101	—	INB	—	INA
0110	—	INB	INB	—
0111	—	INB	—	INB
1000	INA	—	INA	—
1001	INA	—	—	INA
1010	INA	—	INB	—
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1111	—	INA	—	INB

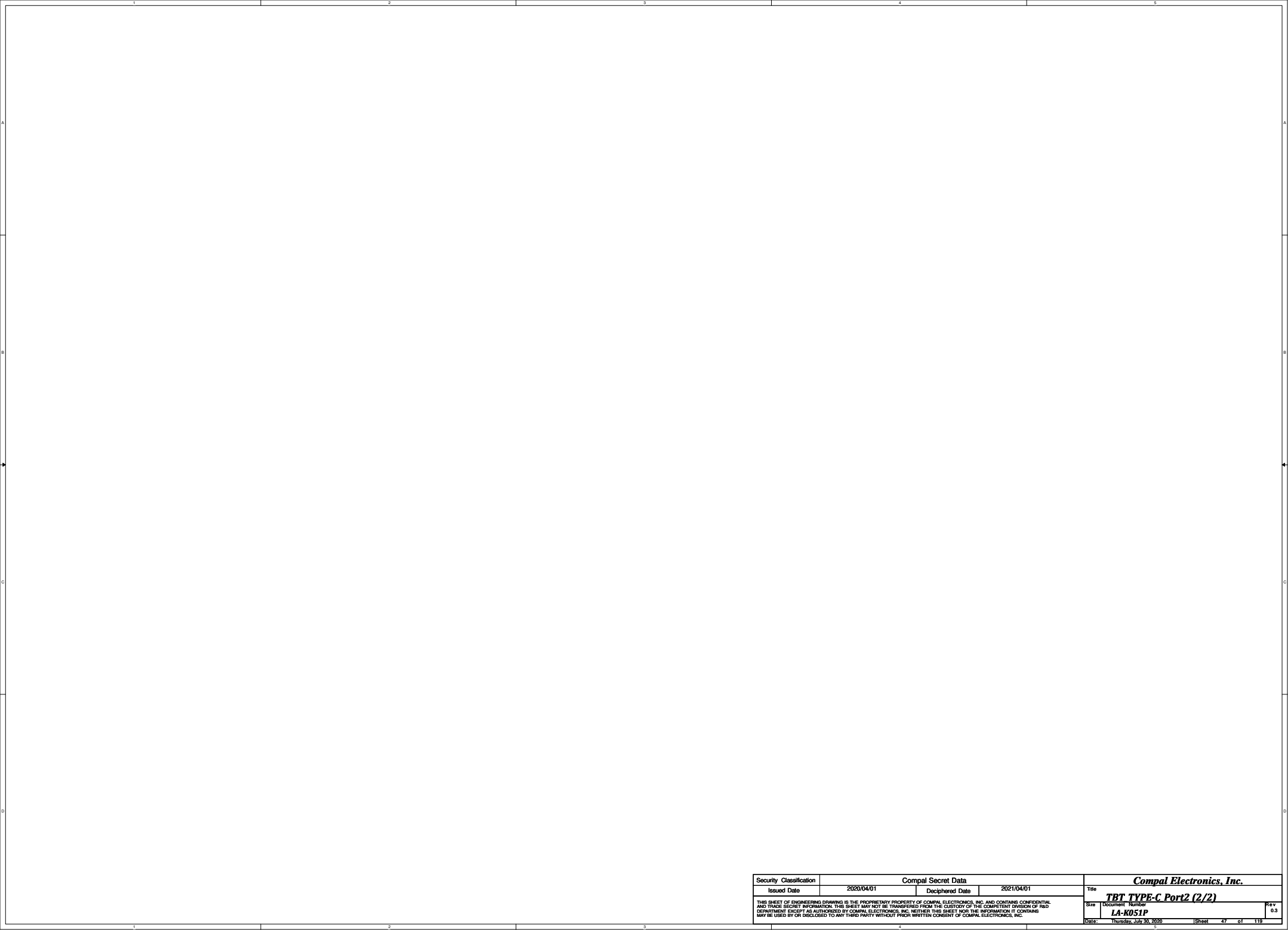




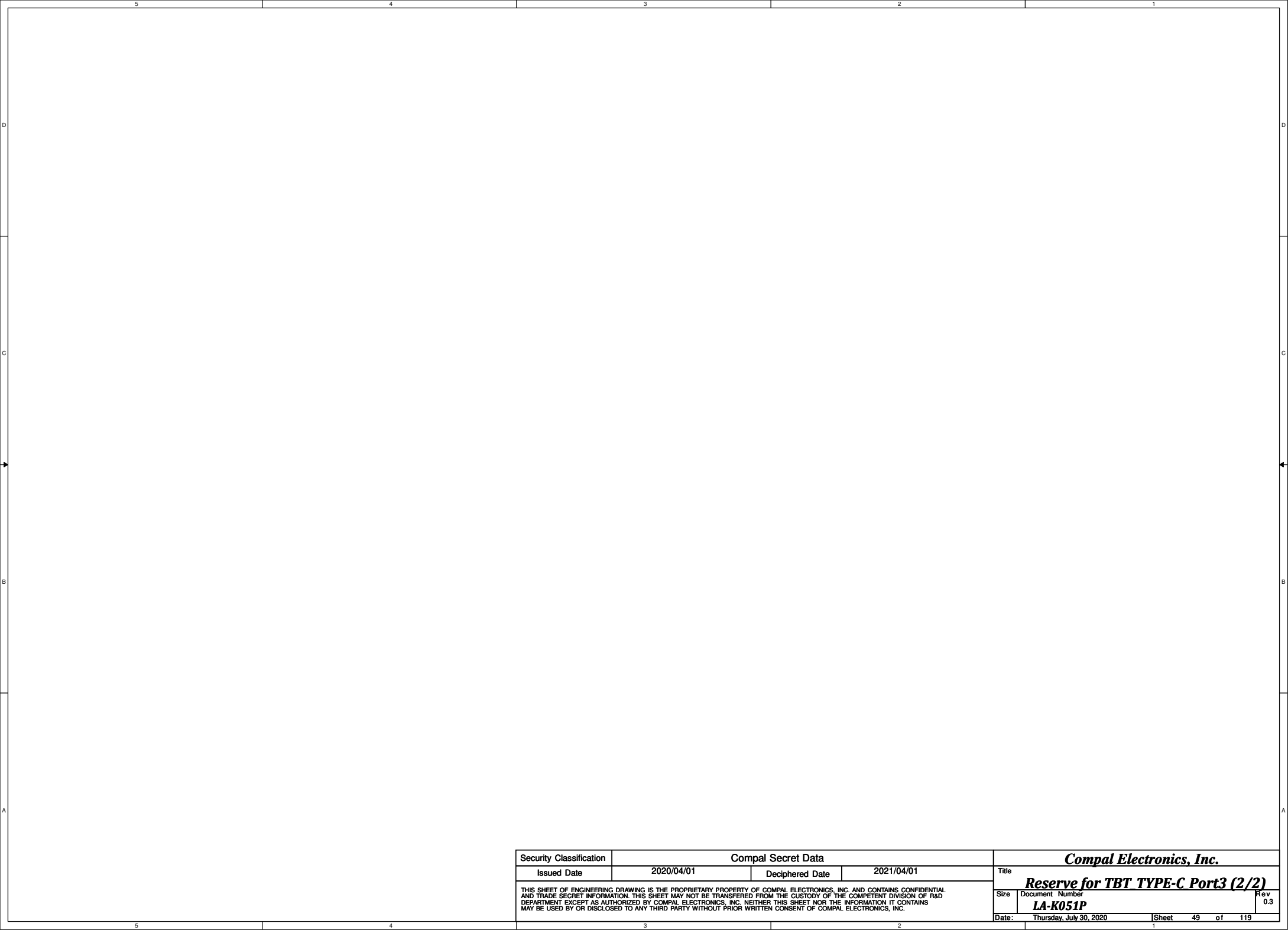
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								Size		Document Number		Rev	
								LA-K051P				0.3	
								Date:		Thursday, July 30, 2020		Sheet	
												45 of 119	



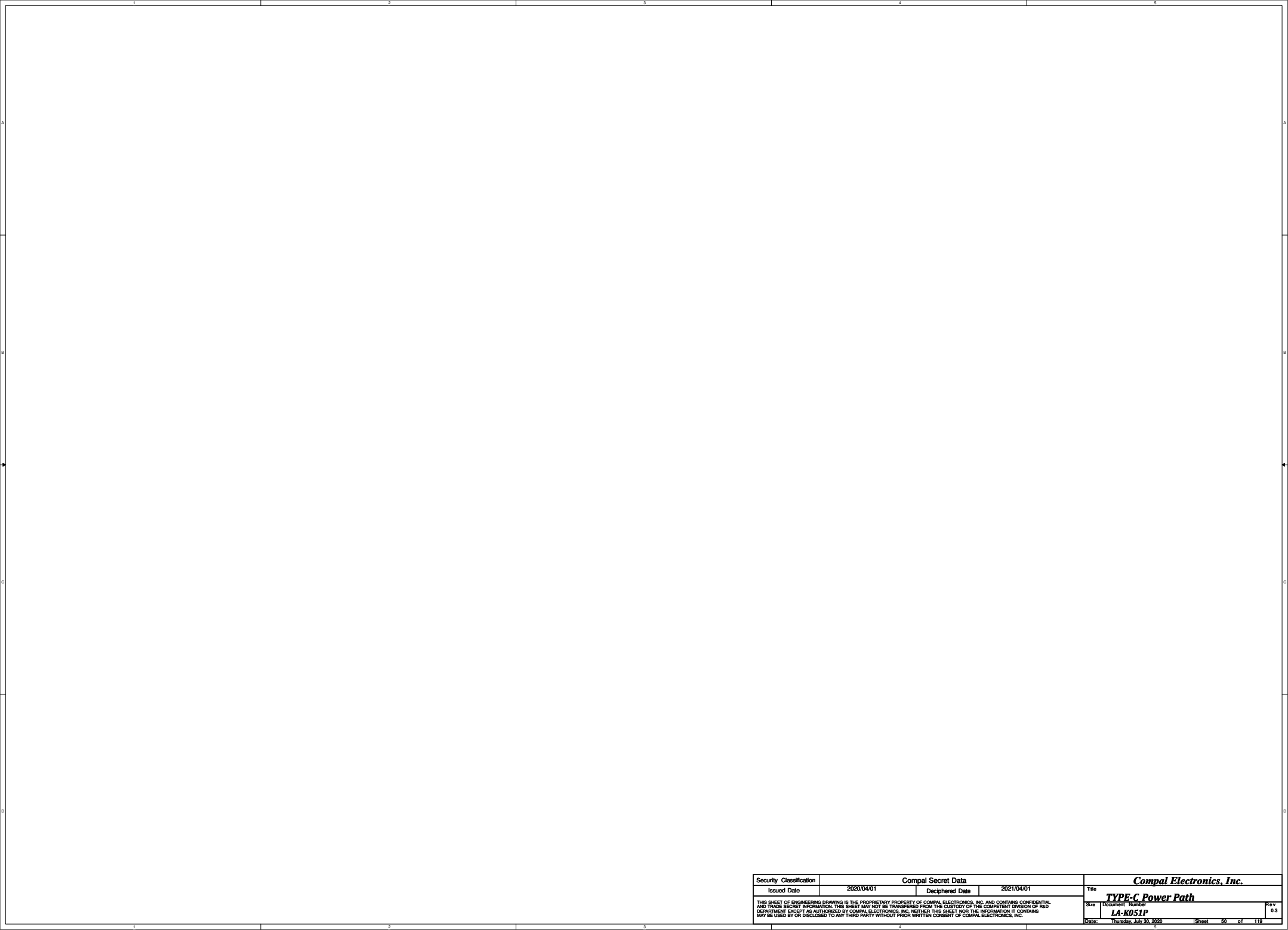
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								Size		Document Number		Rev	
								LA-K051P		0.3			
								Date:		Thursday, July 30, 2020		Sheet	
												46 of 119	



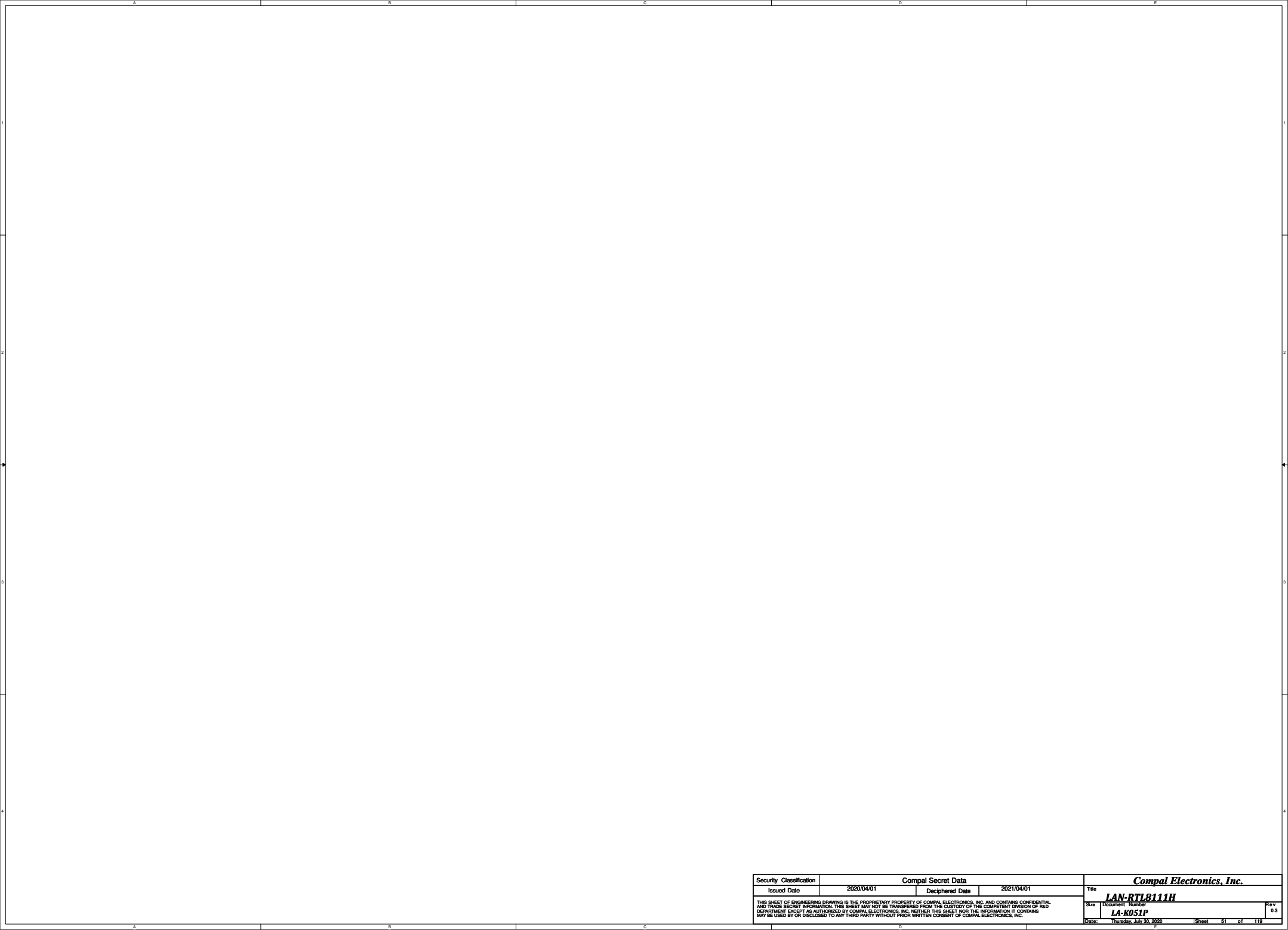
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				LA-K051P	Rev 0.3
Date: Thursday, July 30, 2020				Sheet 47	of 119



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								Size		Document Number		Rev	
								LA-K051P				0.3	
								Date:		Thursday, July 30, 2020		Sheet 49 of 119	



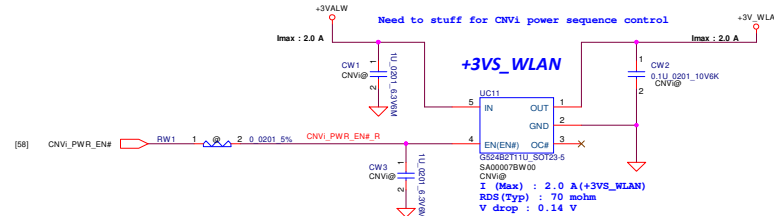
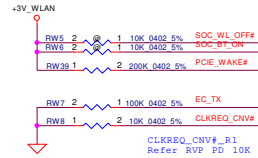
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2020/04/01		2021/04/01		Document Number	
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		Date: Thursday, July 30, 2020		Sheet 50 of 119	



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Date: Thursday, July 30, 2020				Sheet 51 of 119	

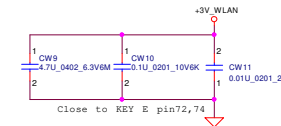
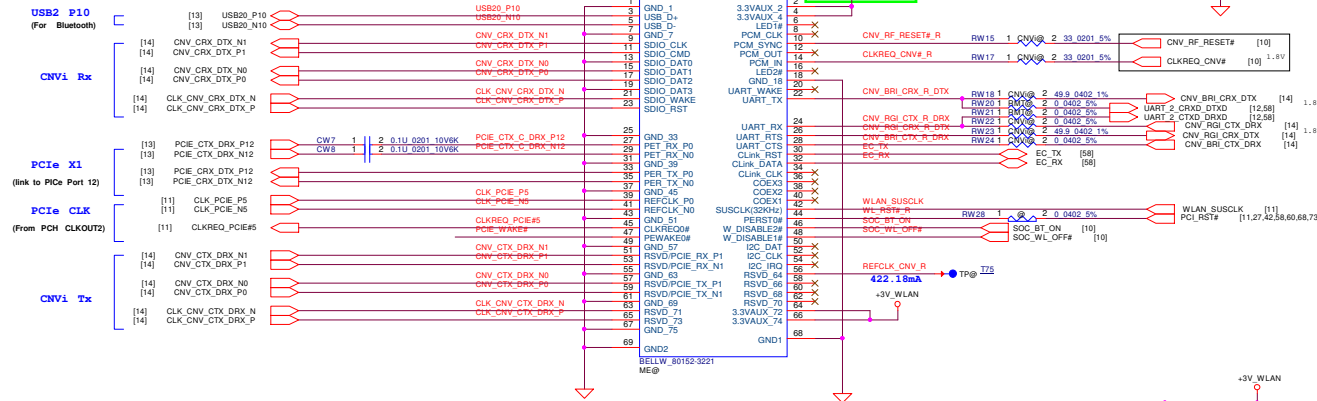
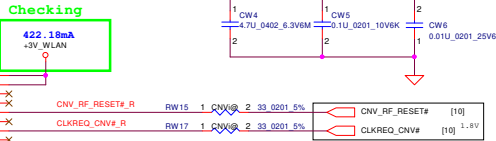


NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNV]



Jefferson Peak:1360mA@peak current
Thunder_Peak:21100mA@peak current

KEY E





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					Reserve for WIGIG/WIDI		
					Size	Document Number	Rev
					LA-K051P		0.3
					Date:		Thursday, July 30, 2020

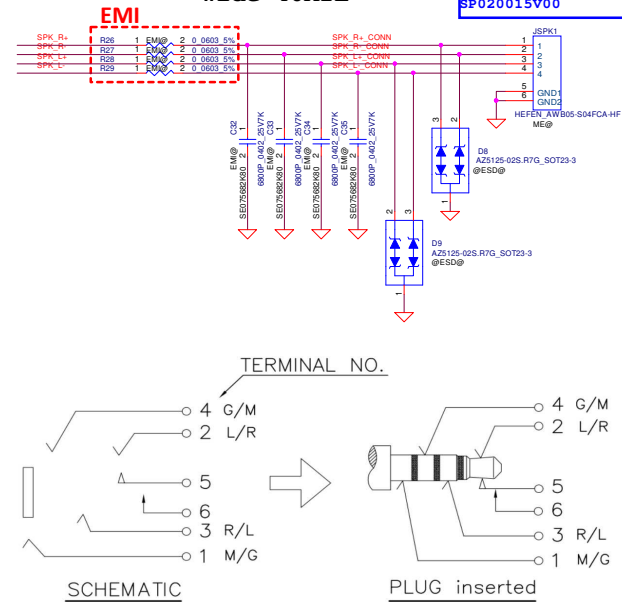
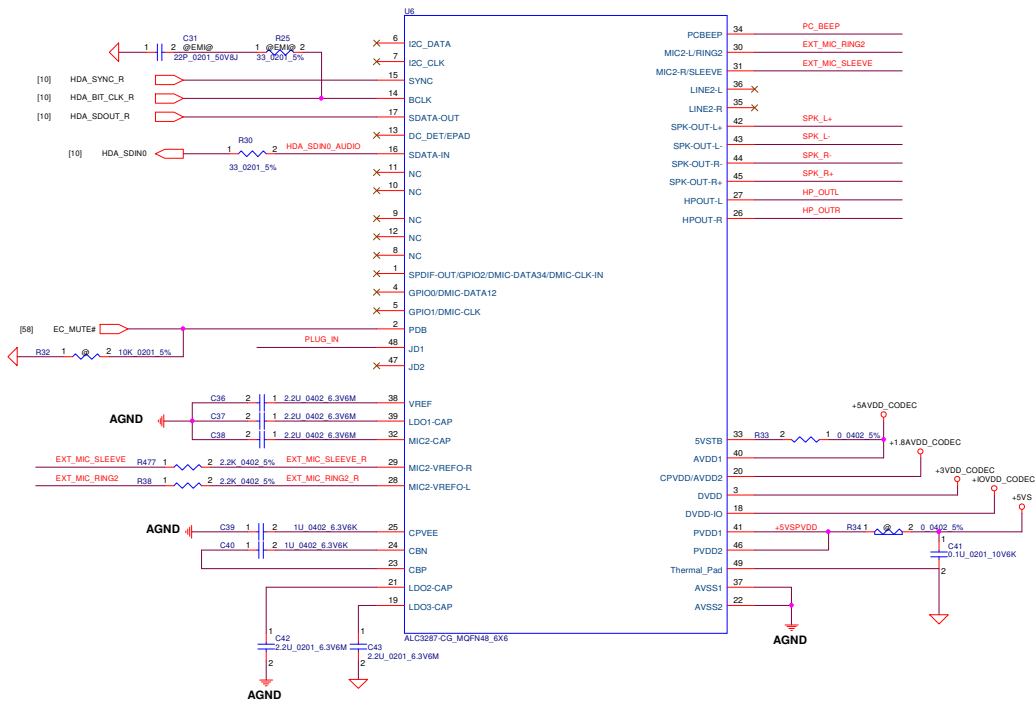


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					Size	Document Number	Rev
						LA-K051P	0.3
					Date:	Thursday, July 30, 2020	Sheet 54 of 119

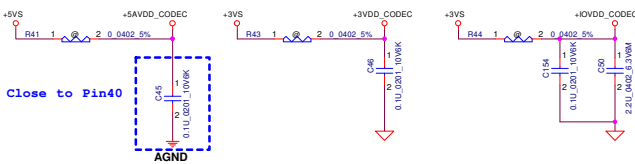


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								Size		Document Number		Rev	
								LA-K051P		0.3			
								Date:		Thursday, July 30, 2020		Sheet 55 of 119	

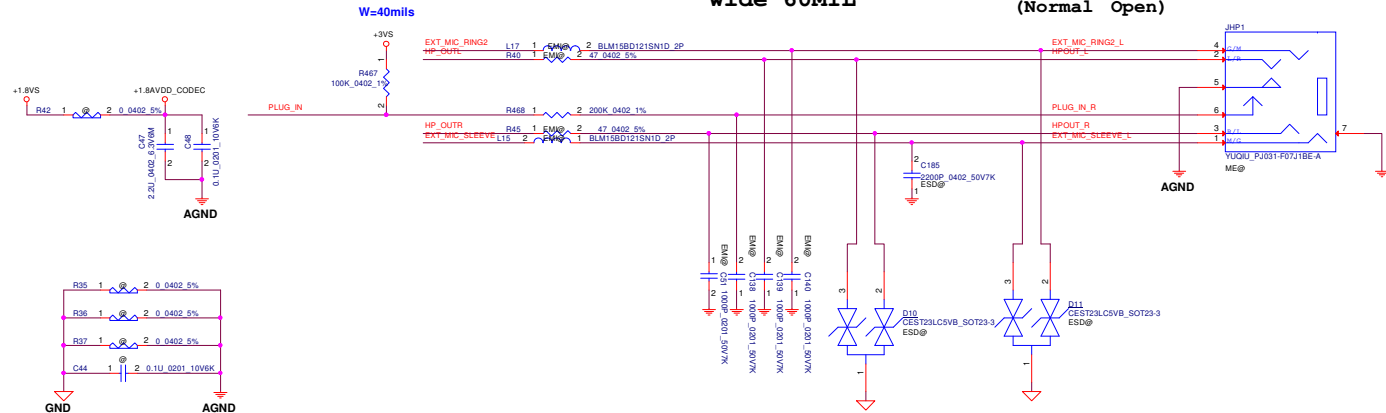
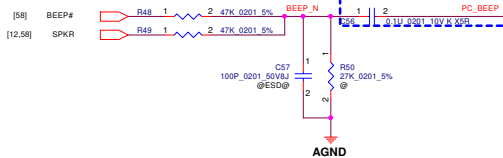
wide 40MIL

Speaker Connector PN
SP020015V00

wide 60MIL

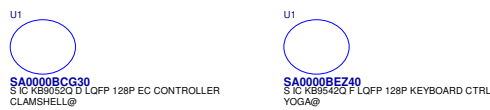
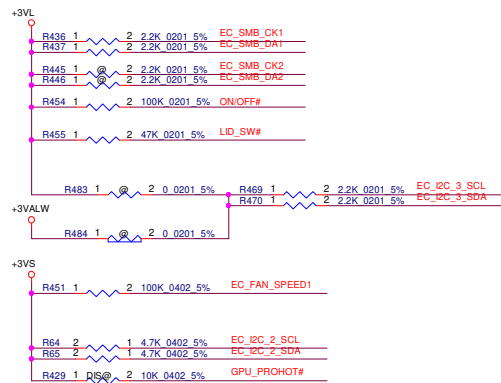
Combo Jack
(Normal Open)For vendor suggest
+SAVDD_CODEC use VS power

PC BEEP

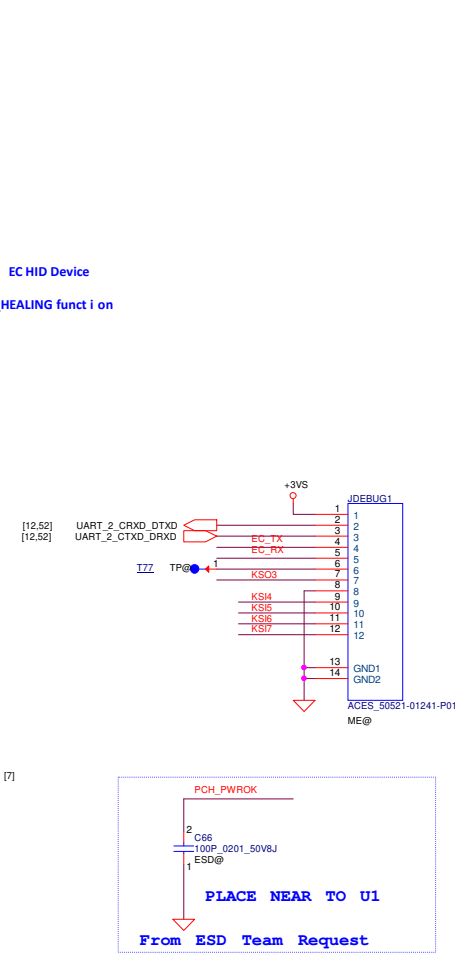
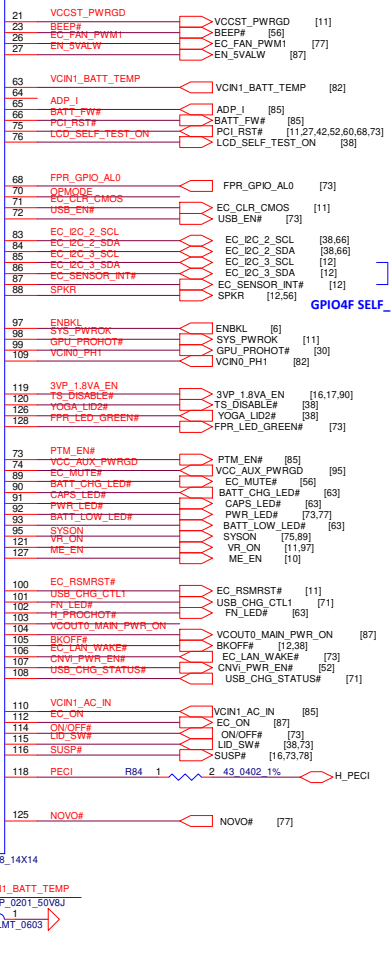
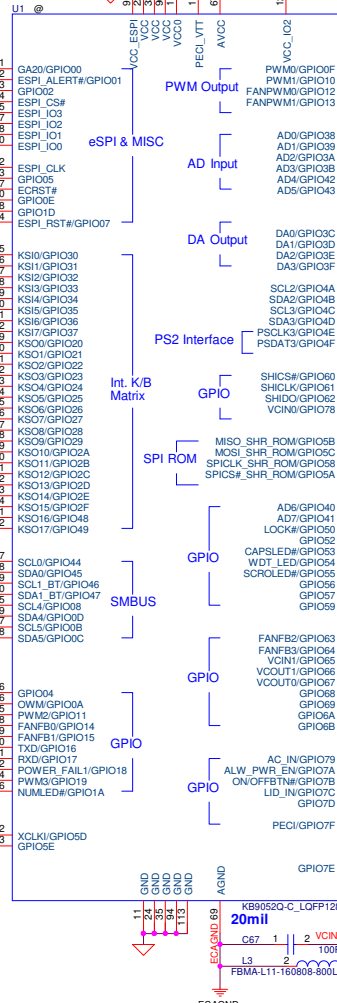
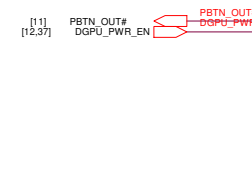
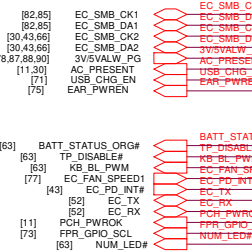
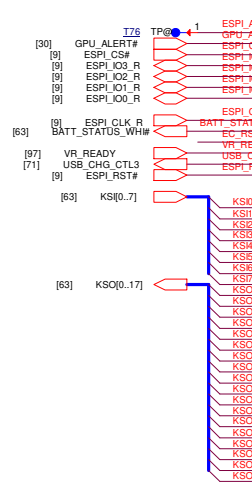
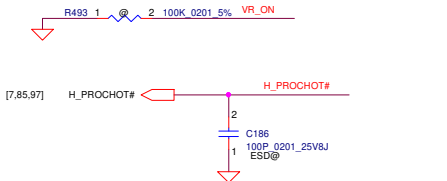
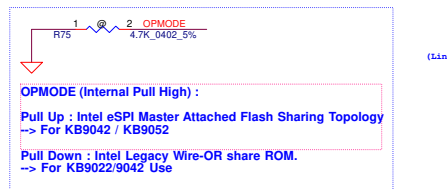
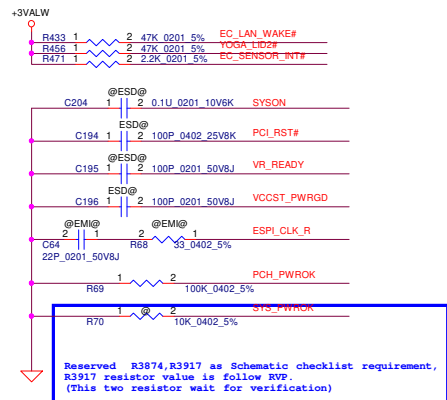




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								Size		Document Number		Rev	
								LA-K051P		0.3			
								Date:		Thursday, July 30, 2020		Sheet 57 of 119	



Pin 1~14 -> 1.8V
Pin1, Pin3 set to OD

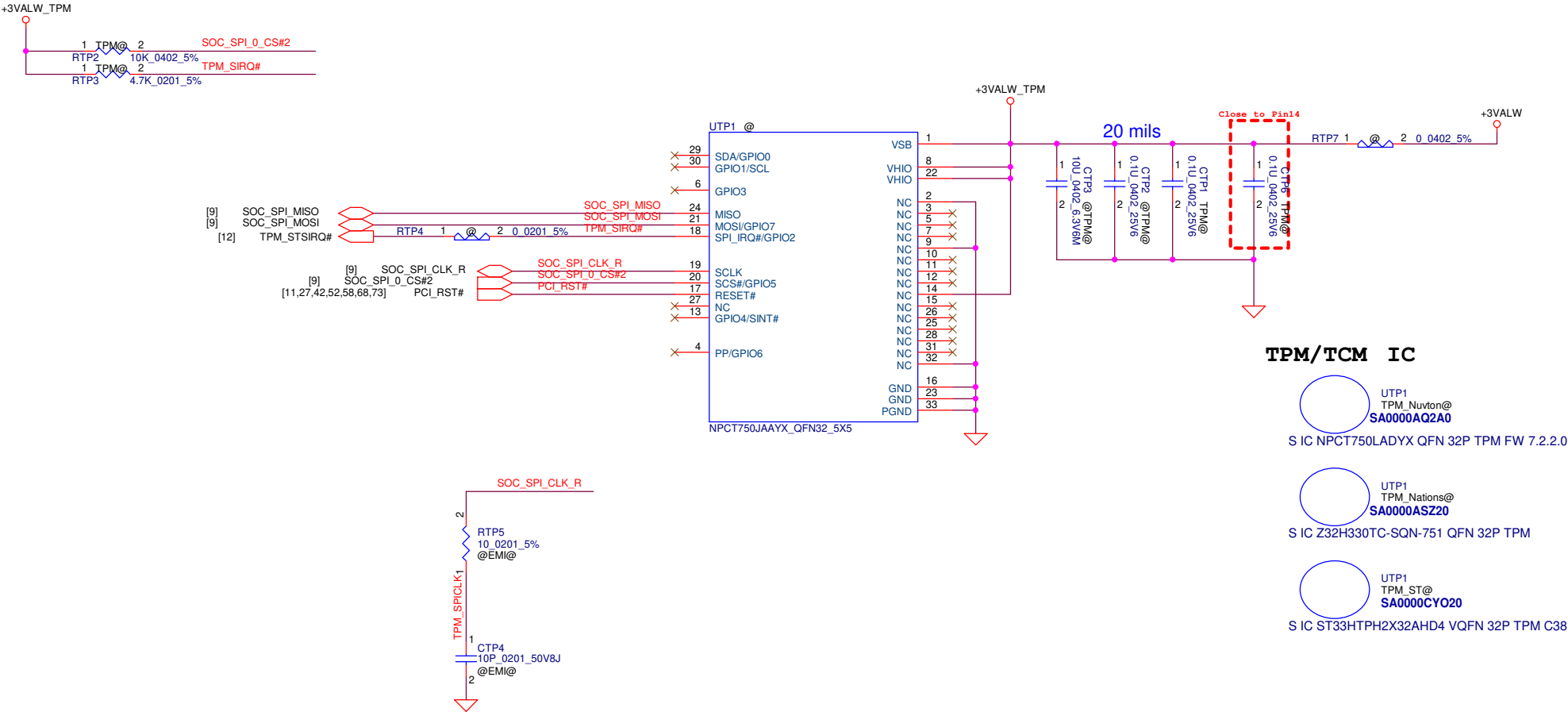




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				Reserve for KBC&SIO				
				Size		Document Number		Rev
				LA-K051P				0.3
				Date:		Thursday, July 30, 2020		Sheet

TPM 2.0 Co-lay

- 1.Nuvton_NPCT750LABYX
- 2.ST_ST33HTPH2E32AAE8
- 3.Nations_Z32H330TC



TPM/TCM IC

UTP1
TPM_Nuvton@
SA0000AQ2A0

S IC NPCT750LADYX QFN 32P TPM FW 7.2.2.0

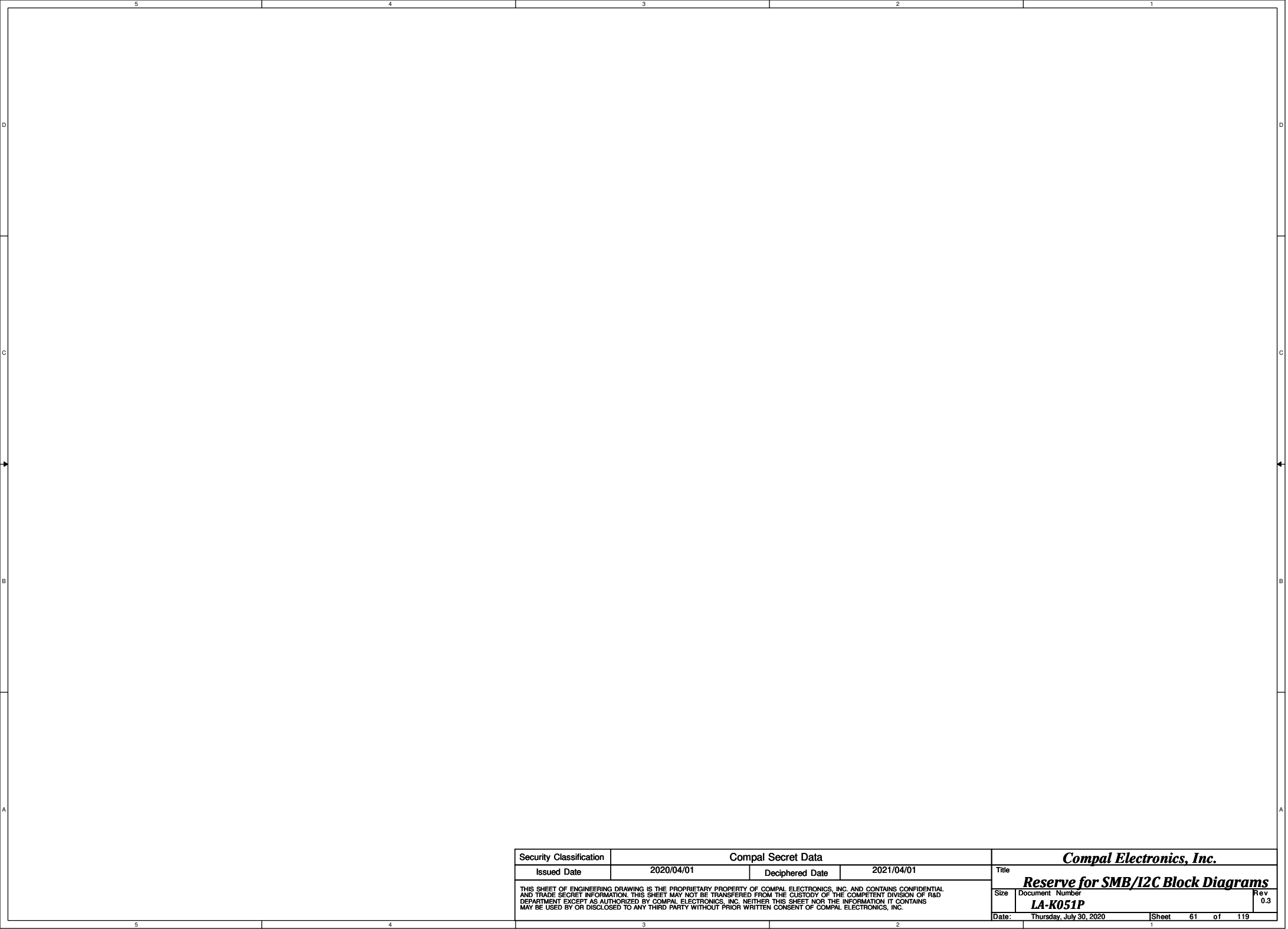
UTP1
TPM_Nations@
SA0000ASZ20

S IC Z32H330TC-SQN-751 QFN 32P TPM

UTP1
TPM_ST@
SA0000CYO20

S IC ST33HTPH2X32AHD4 VQFN 32P TPM C38

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2020/04/01		Deciphered Date		2021/04/01		Title	
										Reserve for Secure & Reset IC	
										Document Number	
										LA-K051P	
										Date:	
										Thursday, July 30, 2020	
										Sheet	
										60 of 119	
										Rev	
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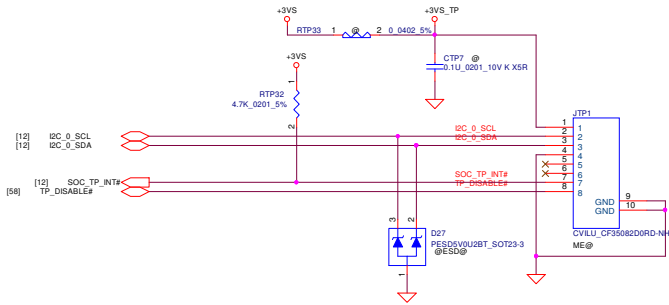


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				Size	Document Number	Rev
				LA-K051P		0.3
				Date: Thursday, July 30, 2020		Sheet 61 of 119

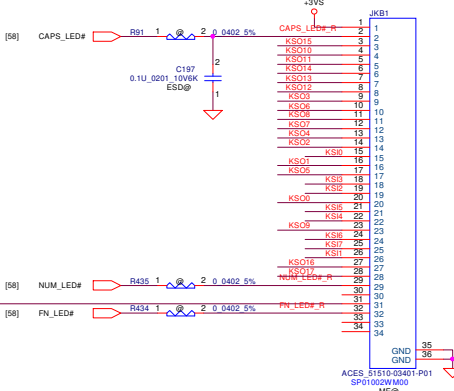


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				Date:	Thursday, July 30, 2020
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Touch Pad

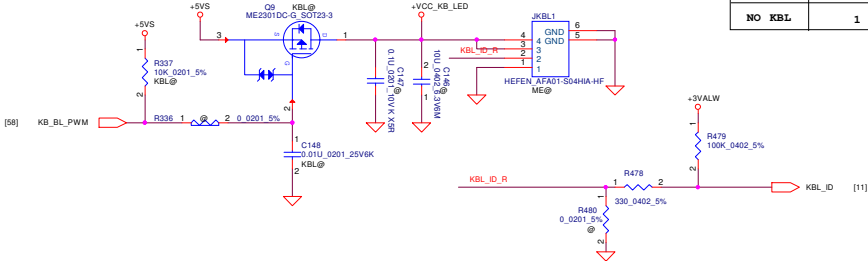


Keyboard

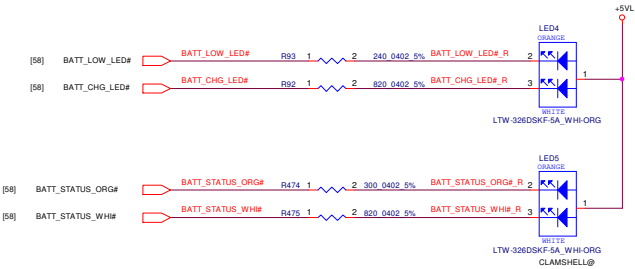


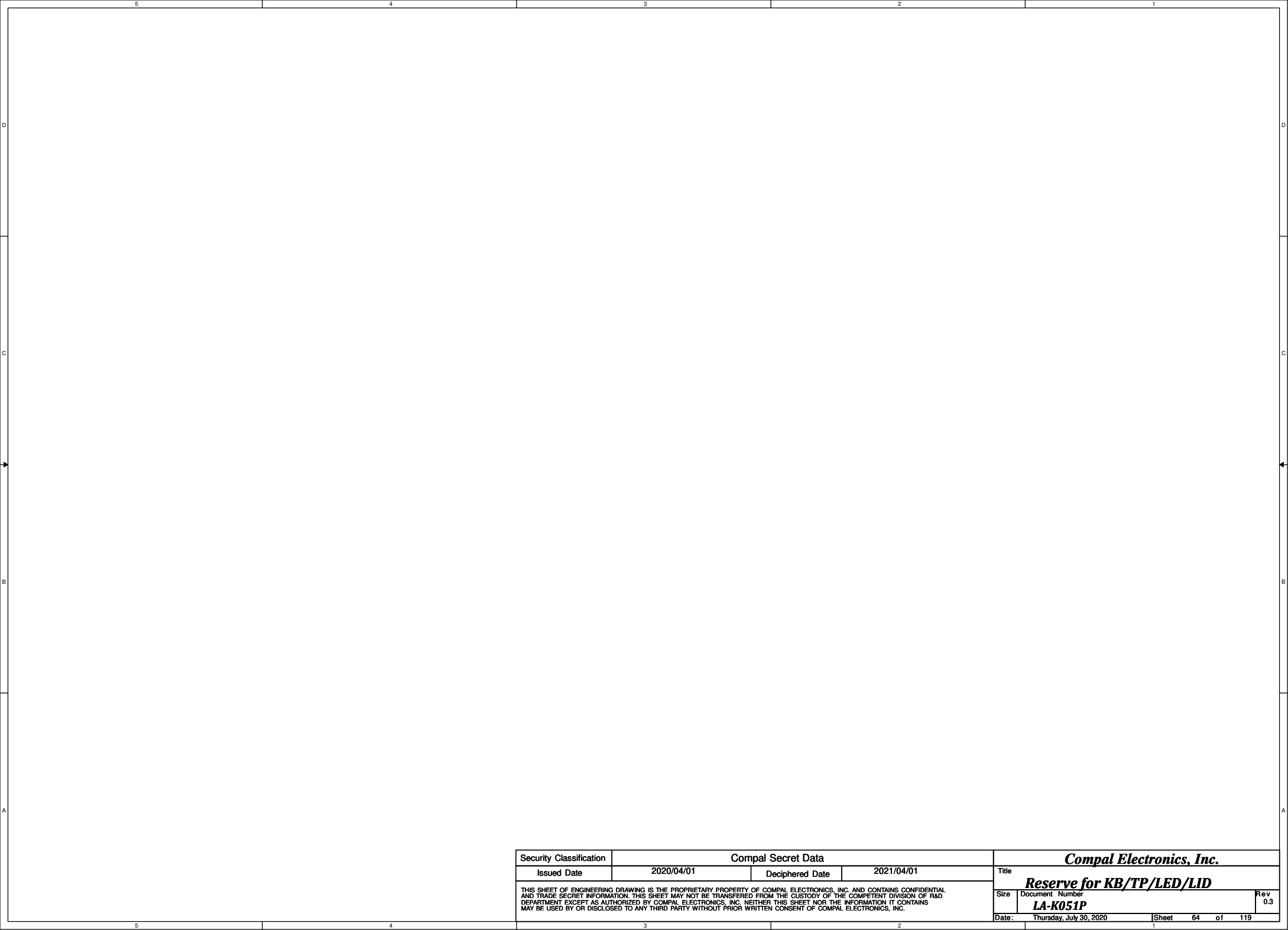
Keyboard Backlight

Function	KBL_ID
KBL	0
NO KBL	1



BATT LED



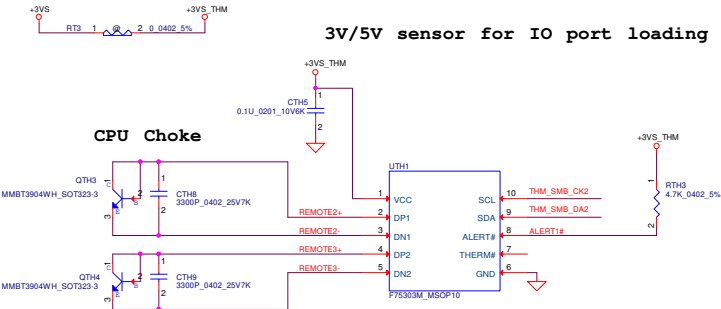


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				Reserve for KB/TP/LED/LID	
				Size	Document Number
				LA-K051P	
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				1	Rev 0.3



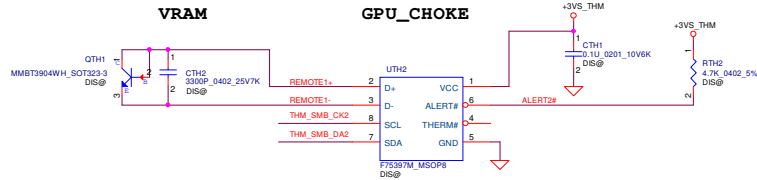
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Issued Date		2020/04/01	Deciphered Date	2021/04/01		Title	
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					Size	Document Number	Rev
					LA-K051P		0.3
					Date:	Thursday, July 30, 2020	Sheet 65 of 119

Thermal sensor

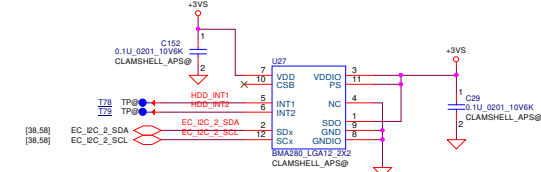


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Charger CHOKE



BMA280 for APS

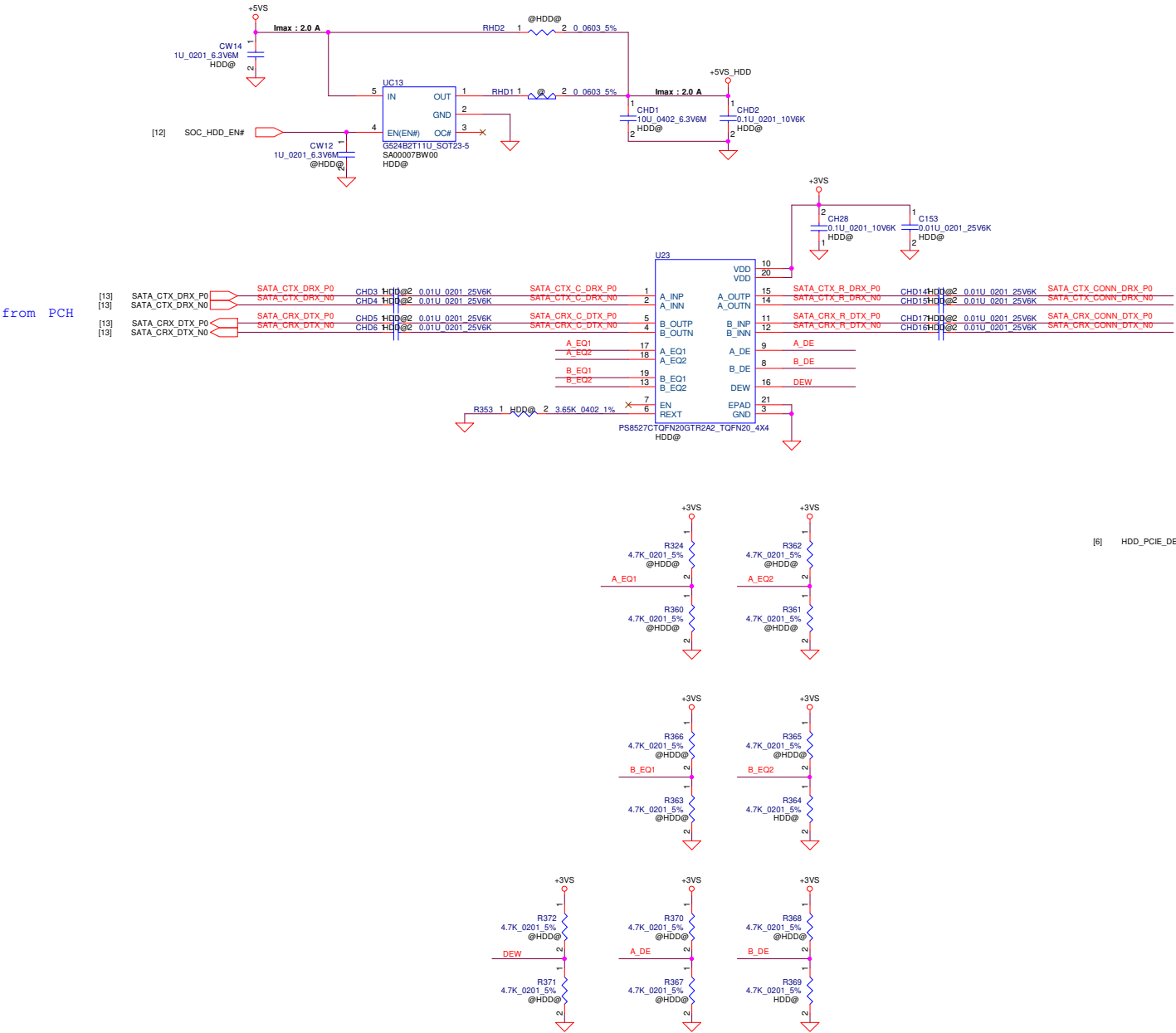


I2C Address: 0x19

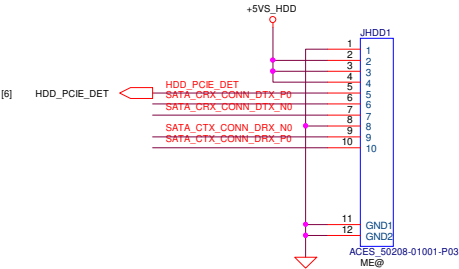
BMA253 for YOGA G-Sensor



SATA HDD

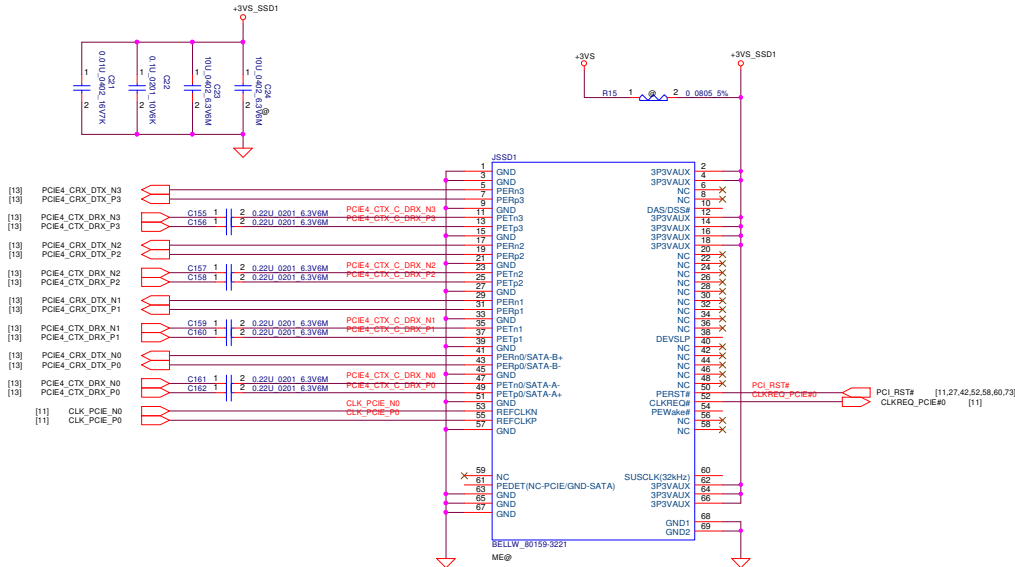


SATA HDD Conn.

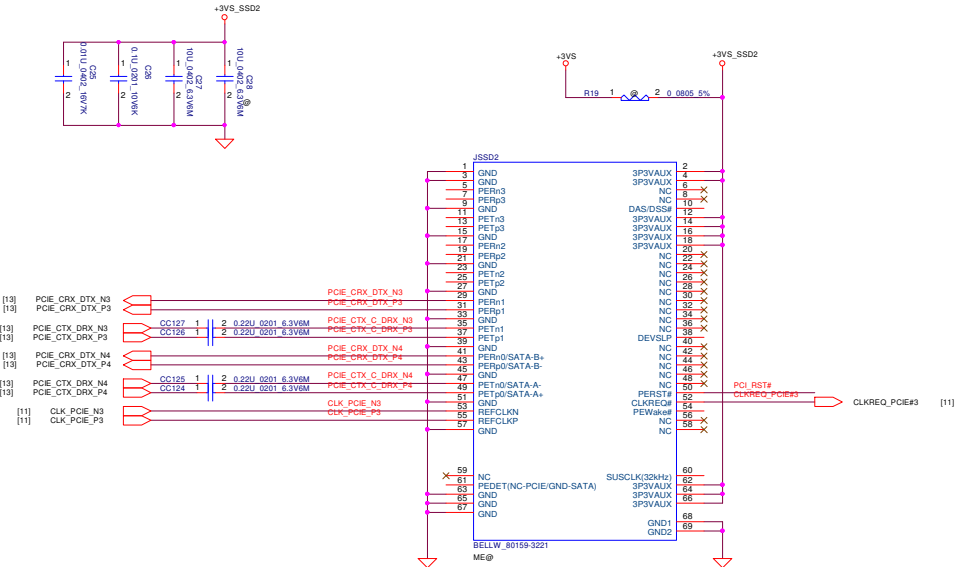


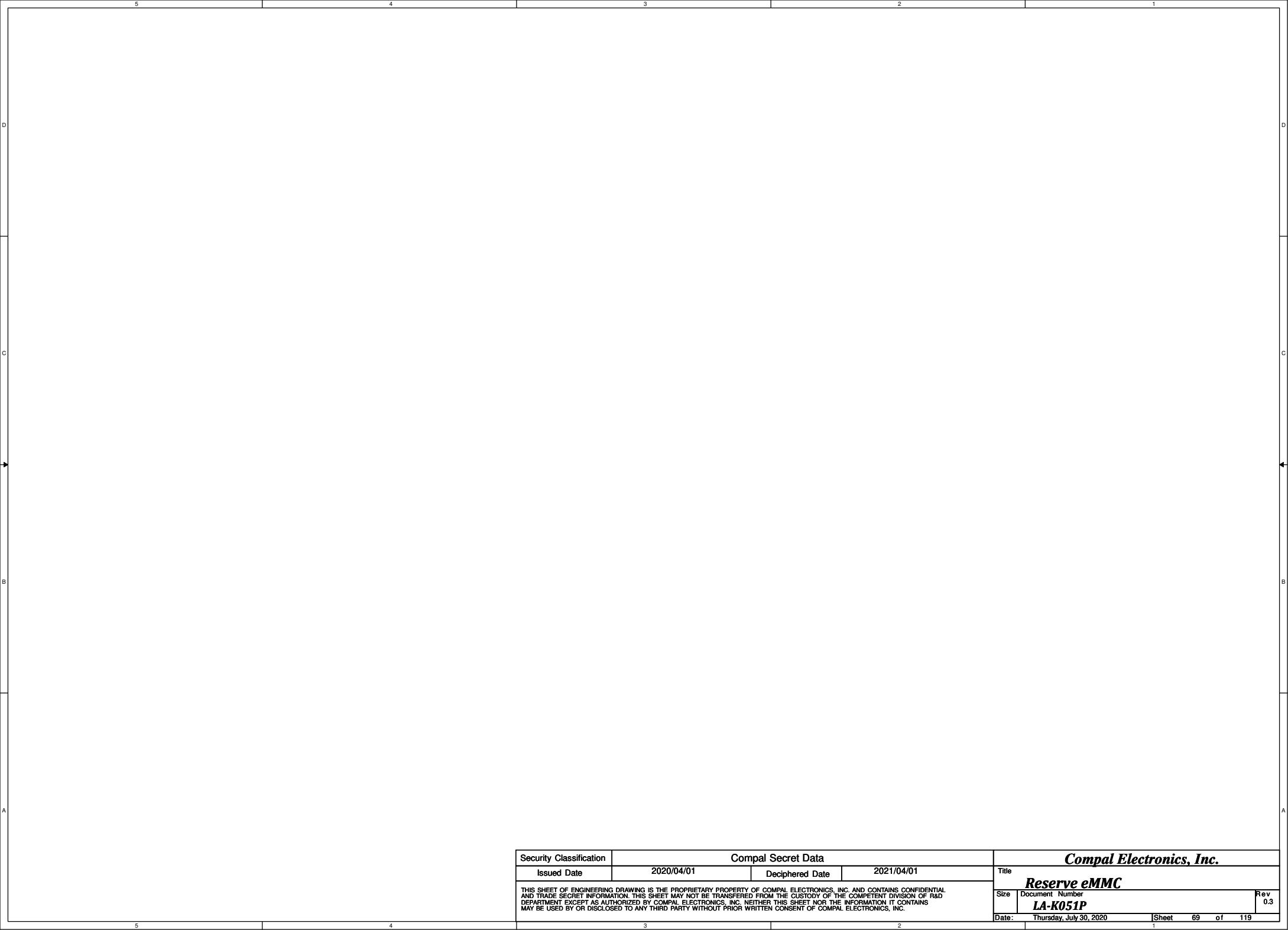
SSD(TYPE M)

SSD PCIE

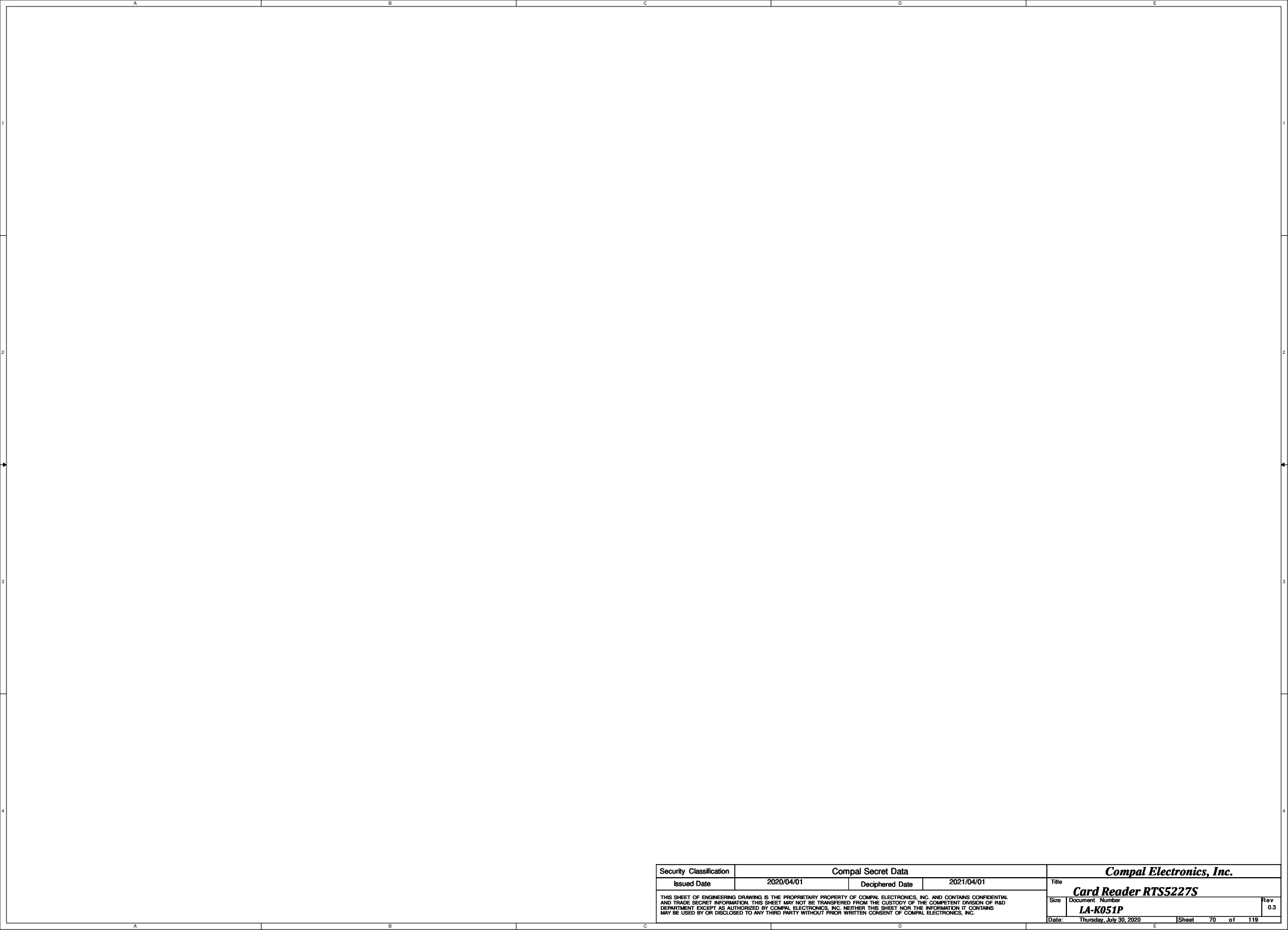


SSD PCIE



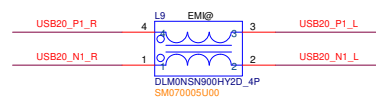
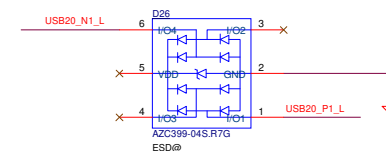
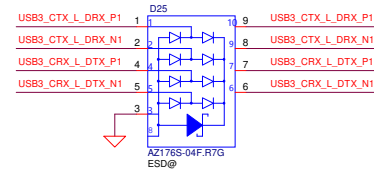
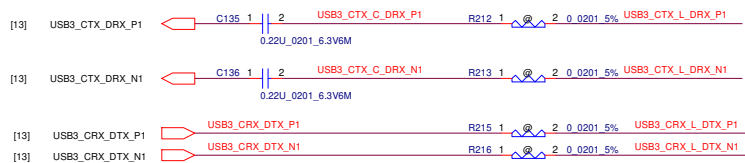
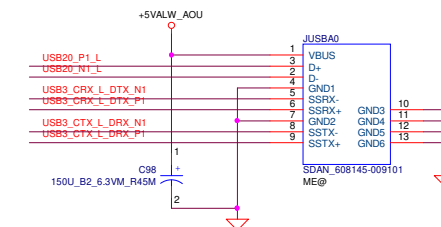
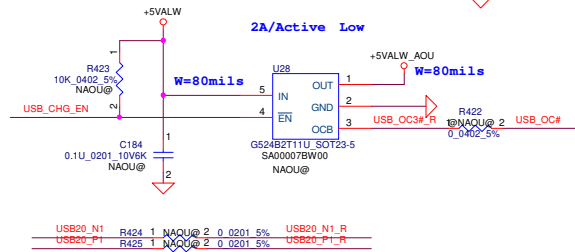
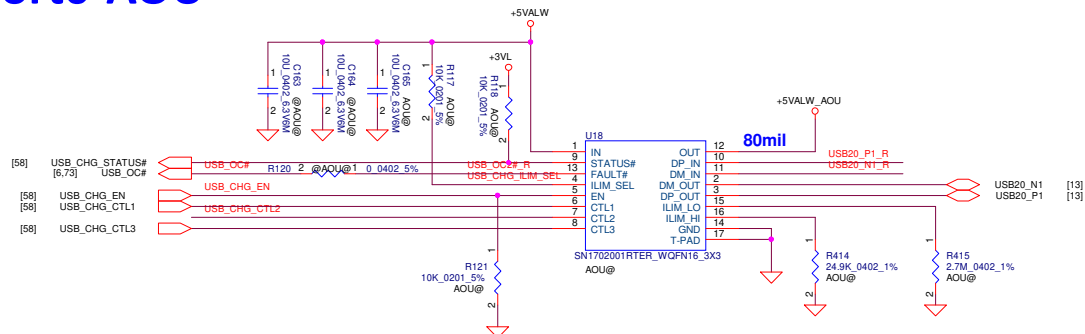


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				Document Number LA-K051P	0.3
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USB3.0_Port0 AOU



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					LA-K051P	0.3
				Date:	Friday, July 31, 2020	Sheet 71 of 119



5 4 3 2 1

D

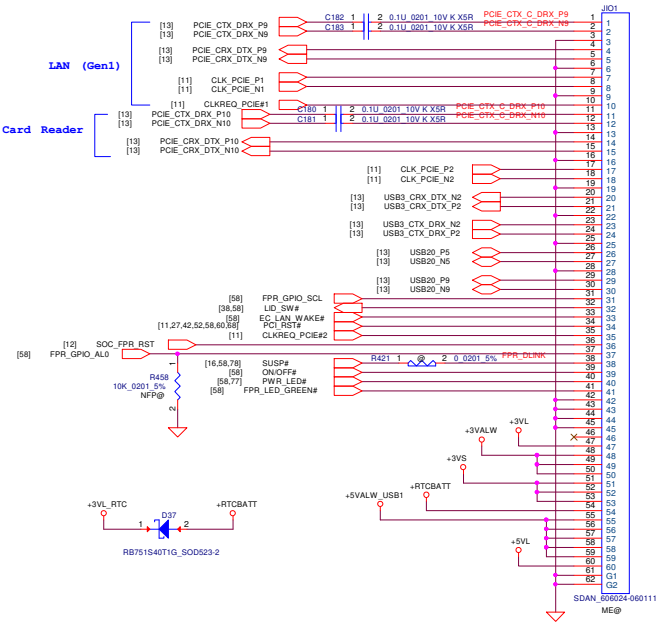
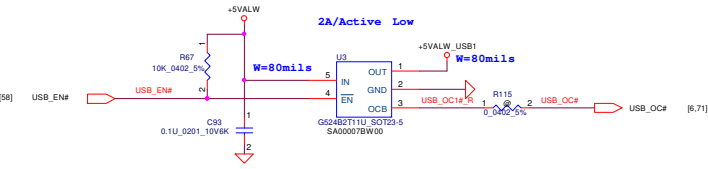
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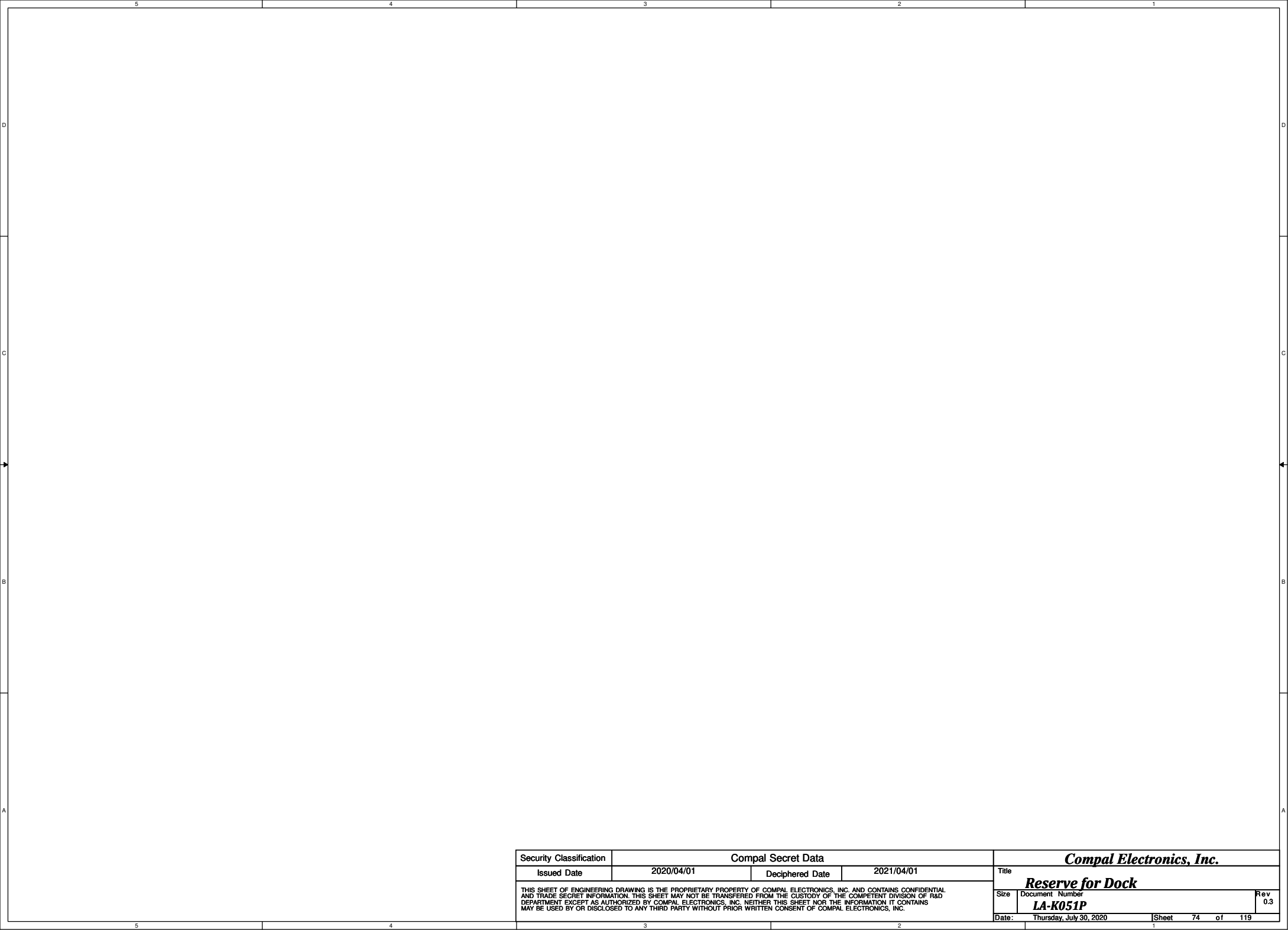
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USB3.0_Port1 SW





5 4 3 2 1

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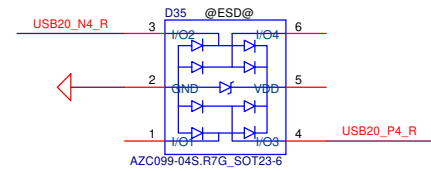
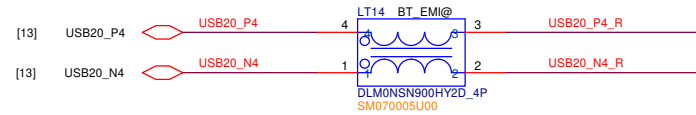
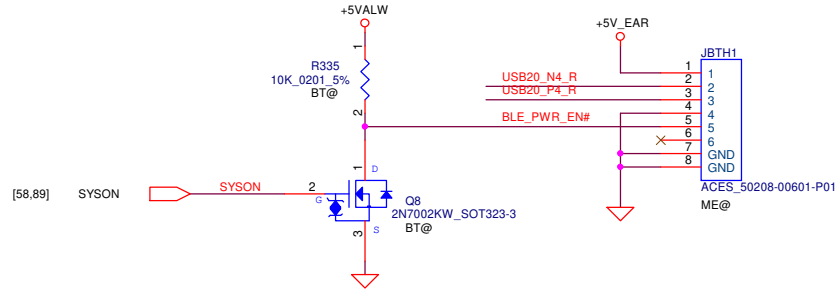
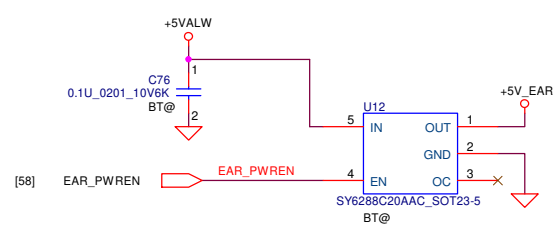
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								Size		Document Number		Rev	
								LA-K051P		0.3			
								Date:		Thursday, July 30, 2020		Sheet 74 of 119	

BT head phone

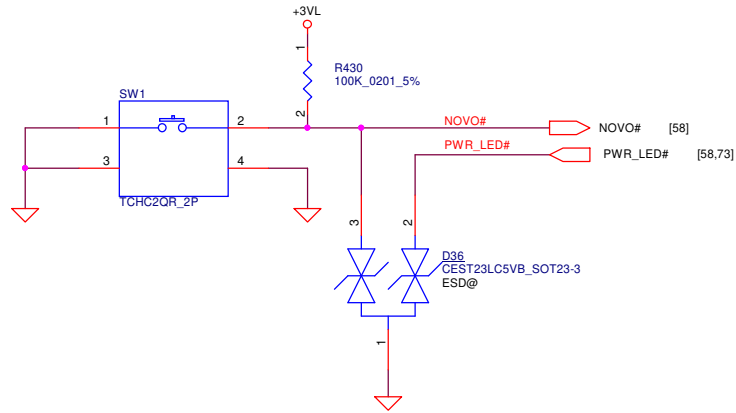


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		Size		Document Number					Rev
				LA-K051P					0.3
		Date: Thursday, July 30, 2020		Sheet		75		of 119	

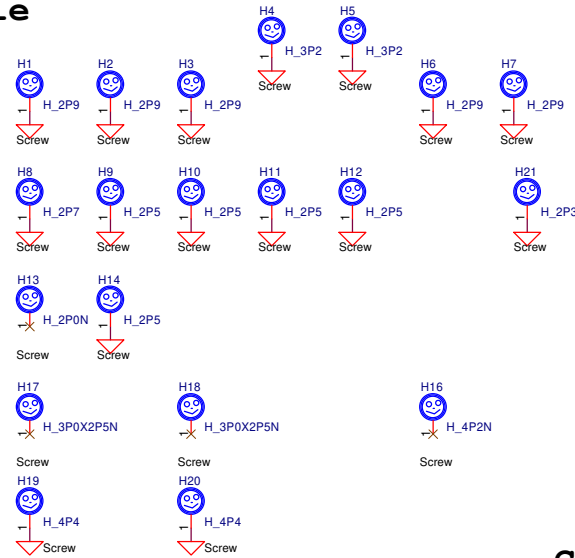


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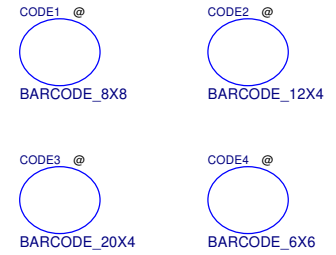
NOVO Button



Screw Hole



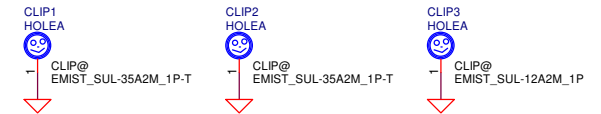
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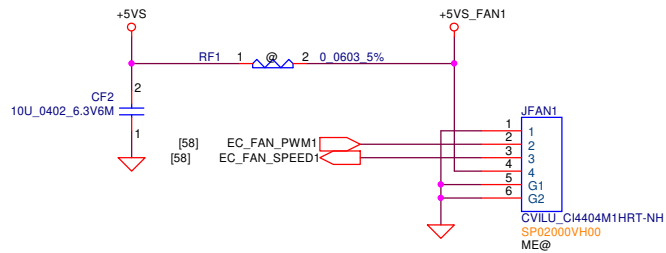
Fiducial Mark



Clip



CPU Fan Control Circuit



ALT. GROUP PARTS DRAM 8G SAM GLV3Y
X7688138LA4
DDR_S8G@



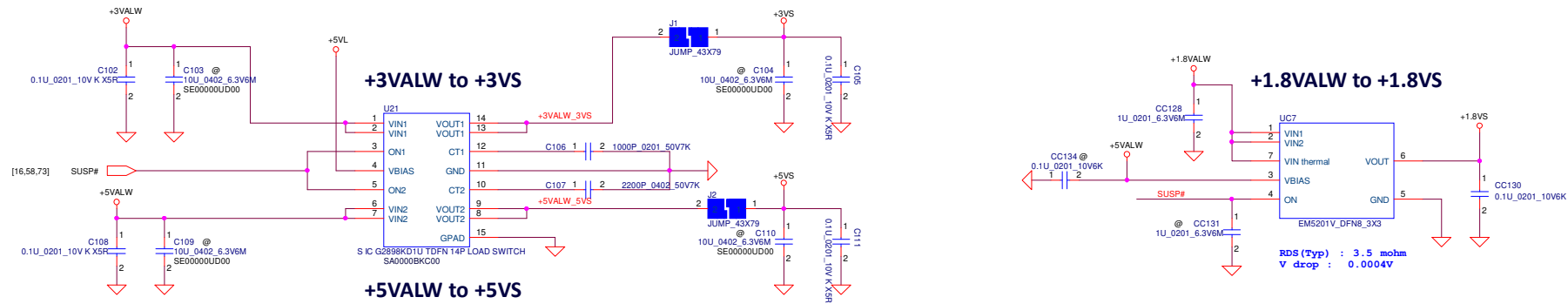
SMT EMC YOGA FOR EE AK051 GLV3Y
X4EAN738L51
ESD@



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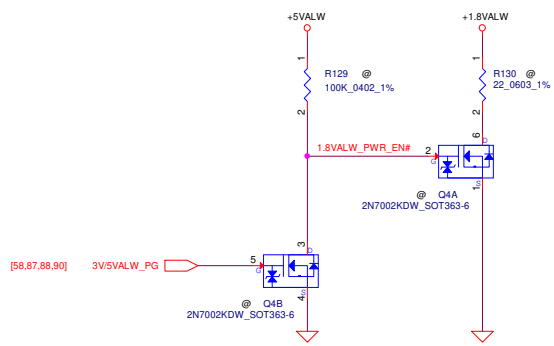
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				Size	Document Number	Rev
				LA-K051P		
				Date:	Thursday, July 30, 2020	Sheet 77 of 119
				Rev 0.3		

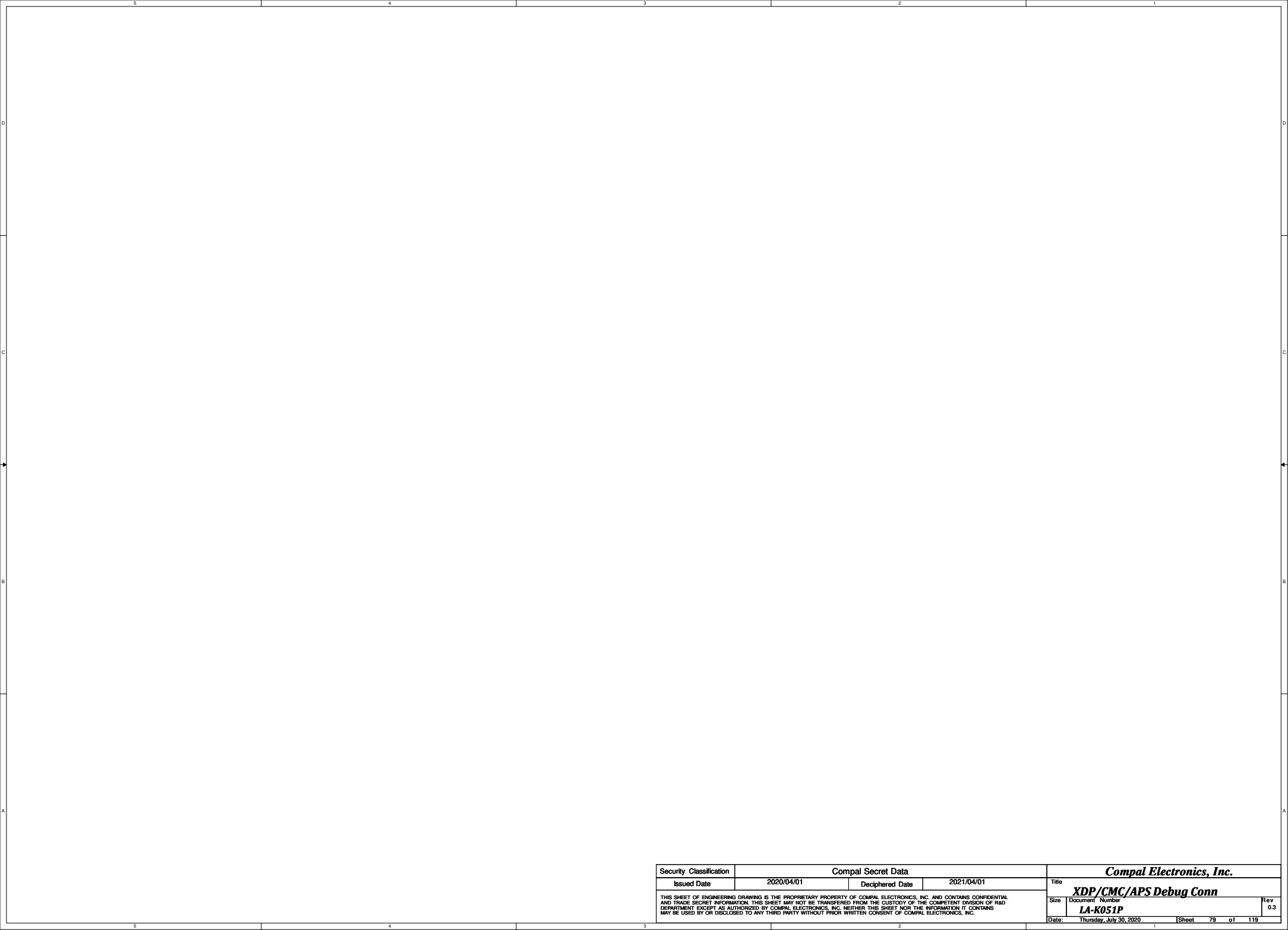
DC to DC



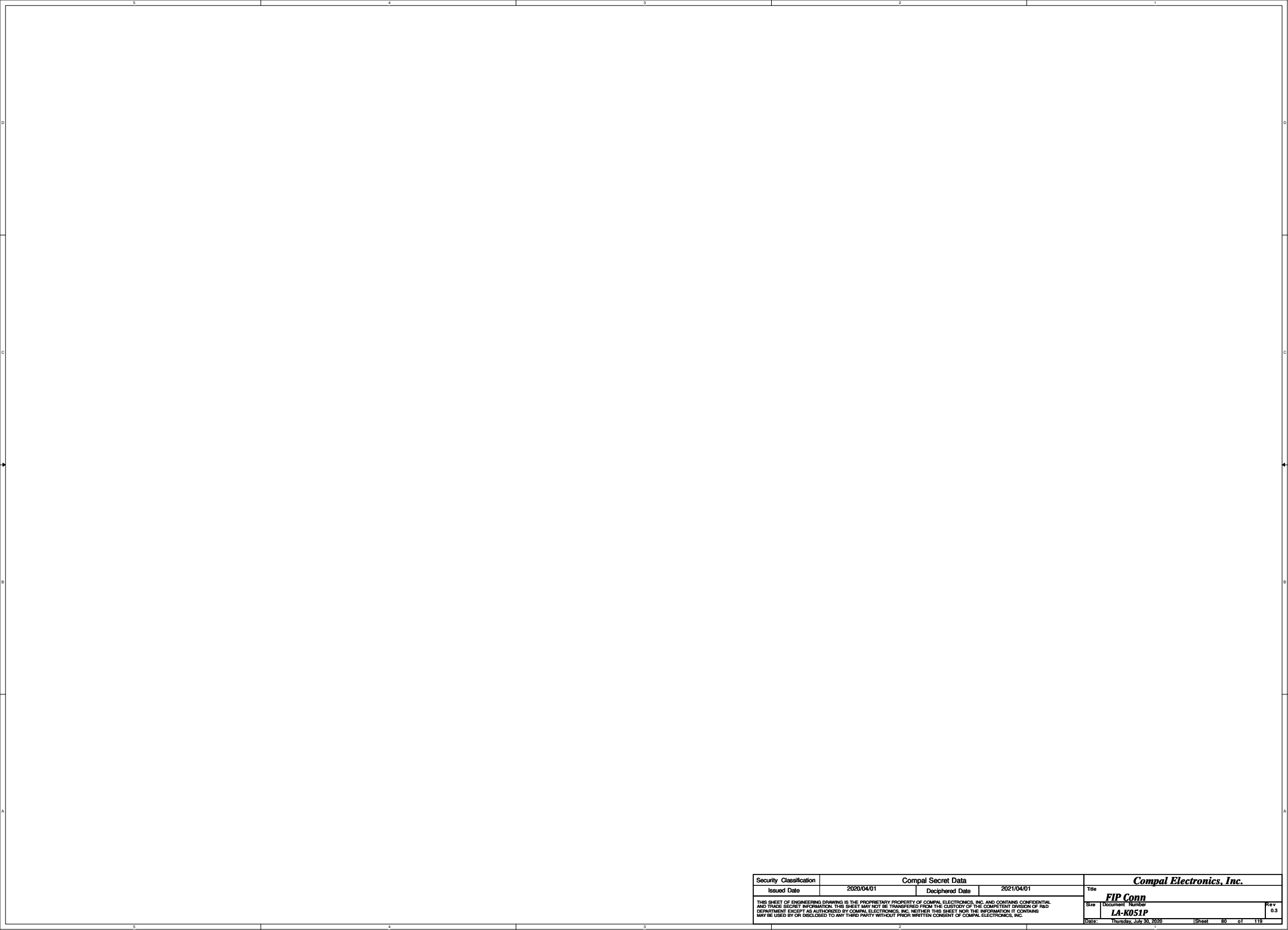
DISCHARGE CIRCUIT

For +1.8VALW Discharge





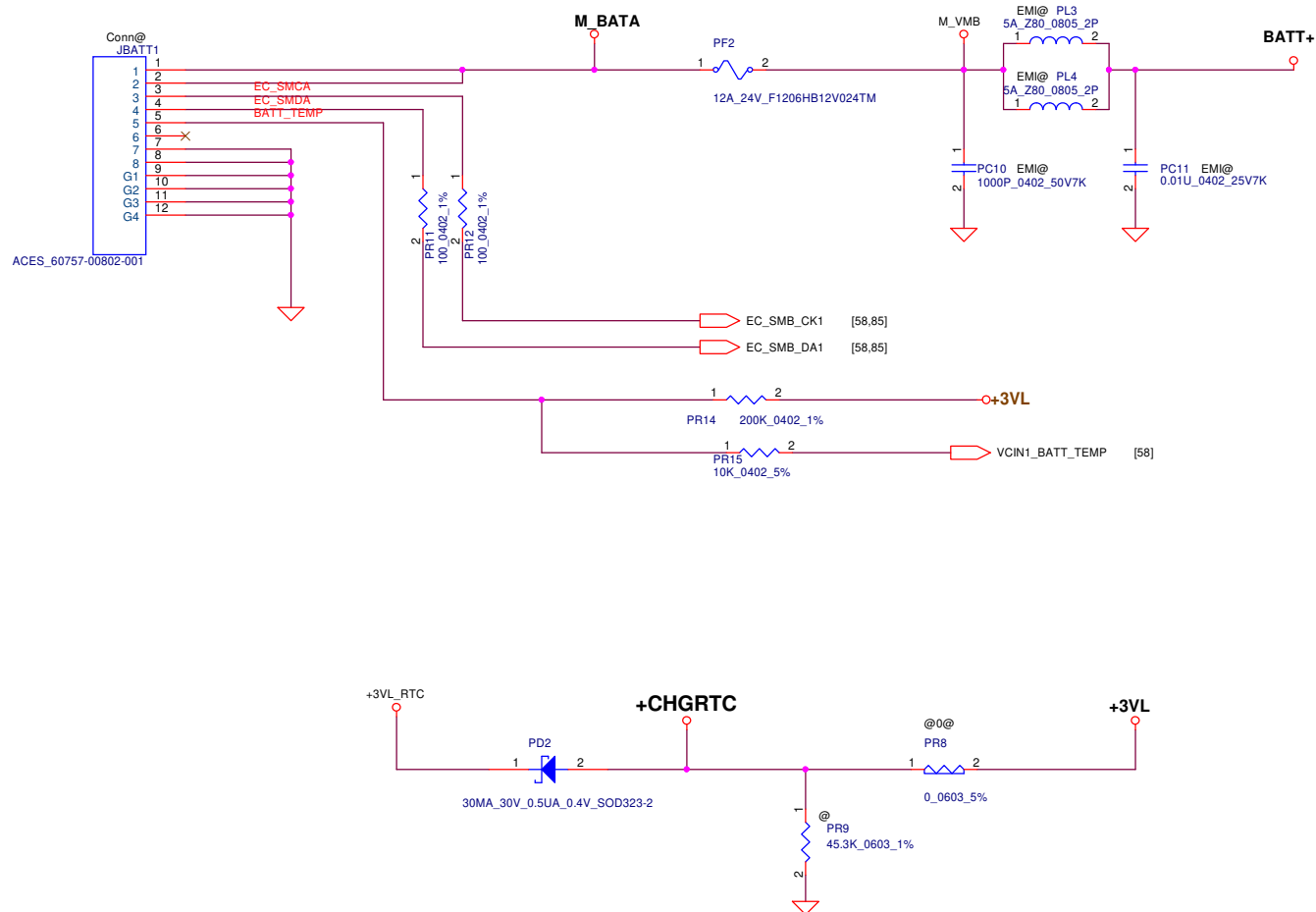
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Date: Thursday, July 30, 2020		1		0.3	
Sheet		79		of 119	



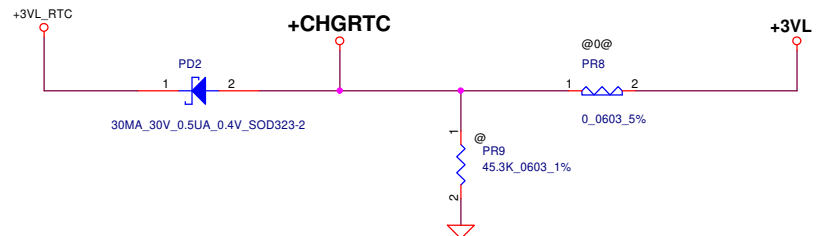
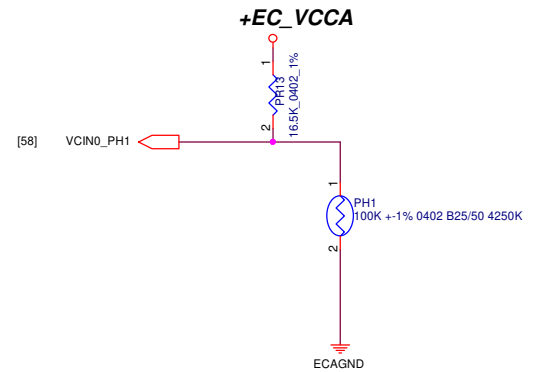
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				LA-K051P	Rev 0.3
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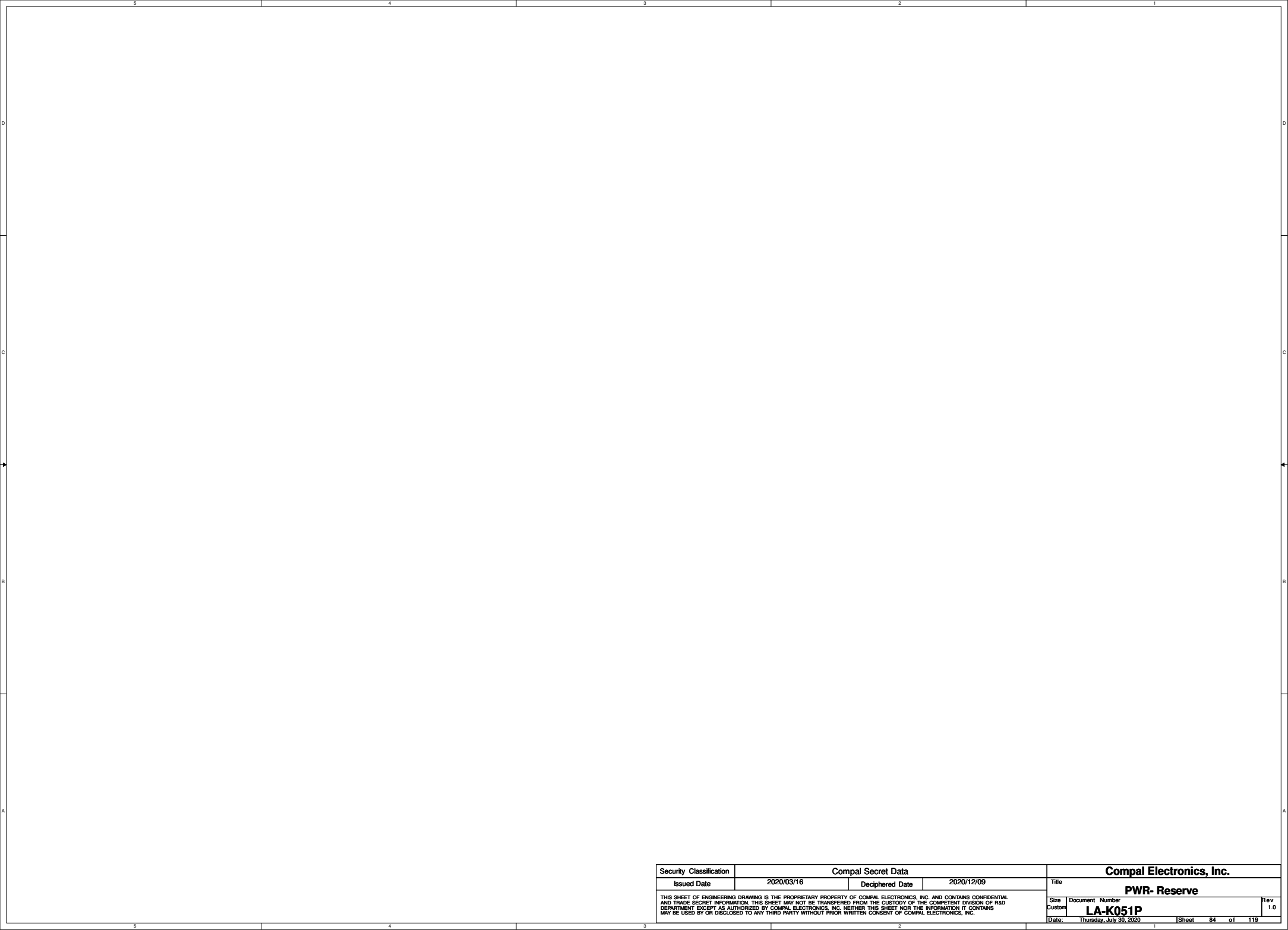
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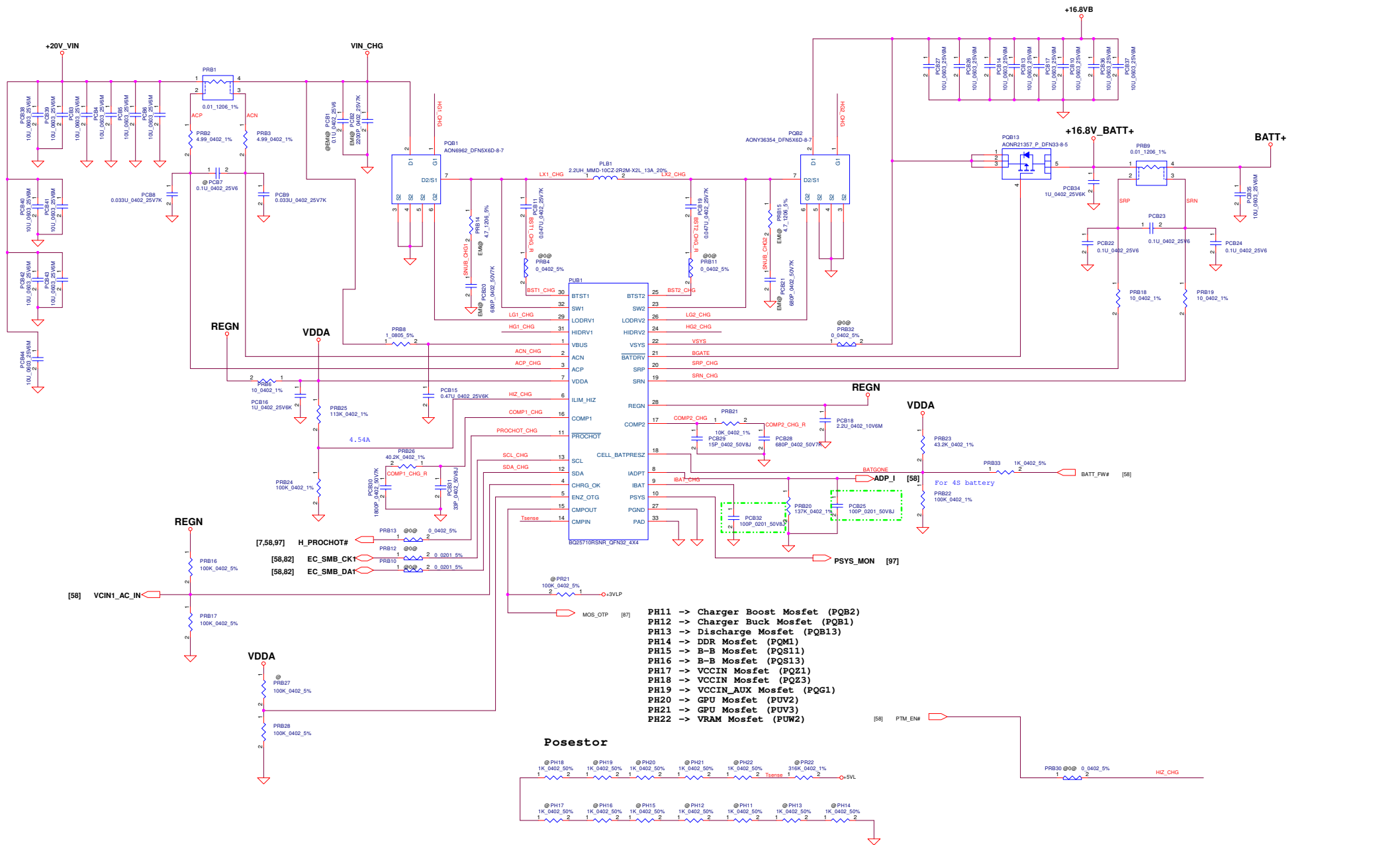
PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

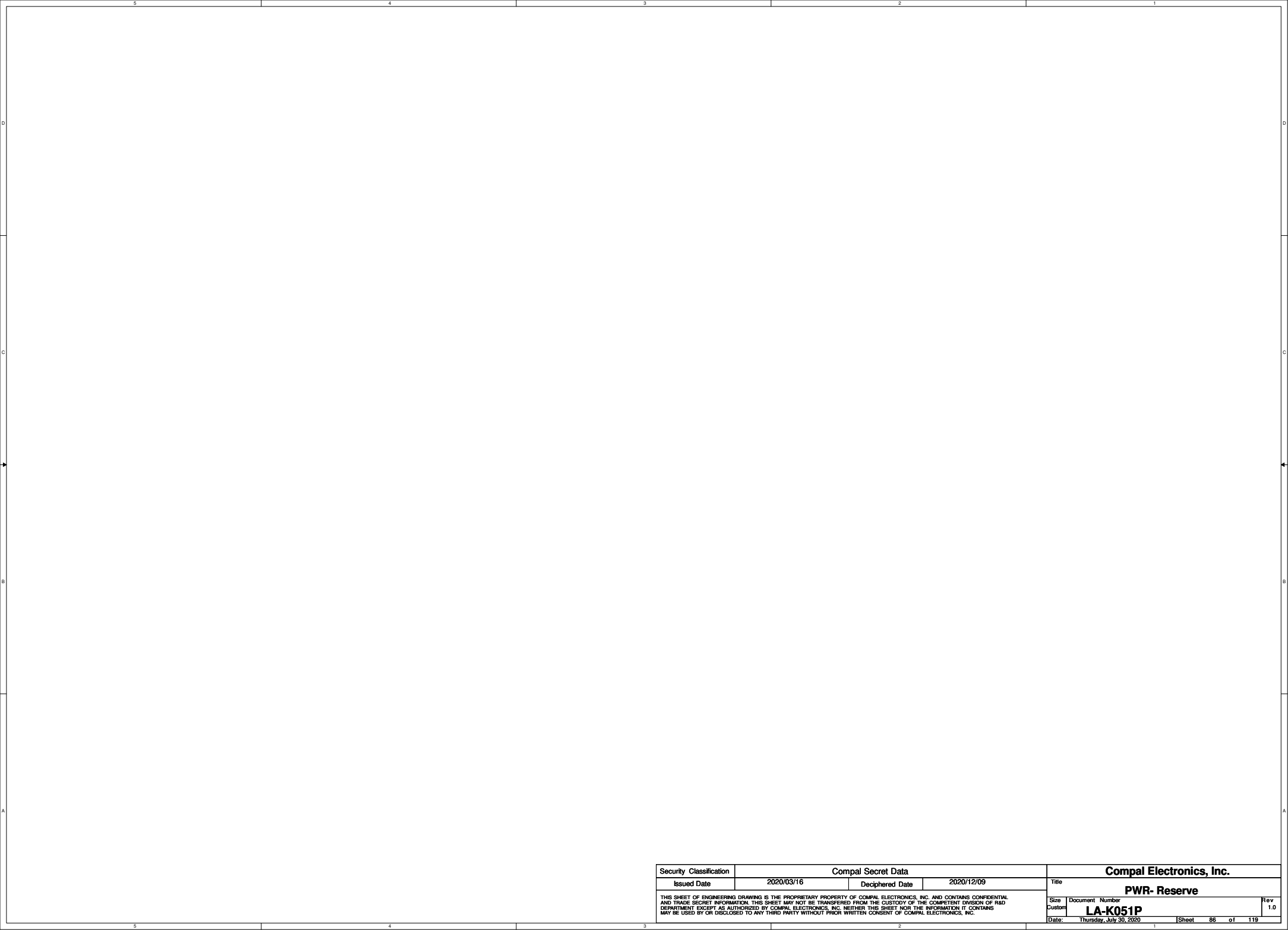


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		LA-K051P		Date:	Friday, July 31, 2020
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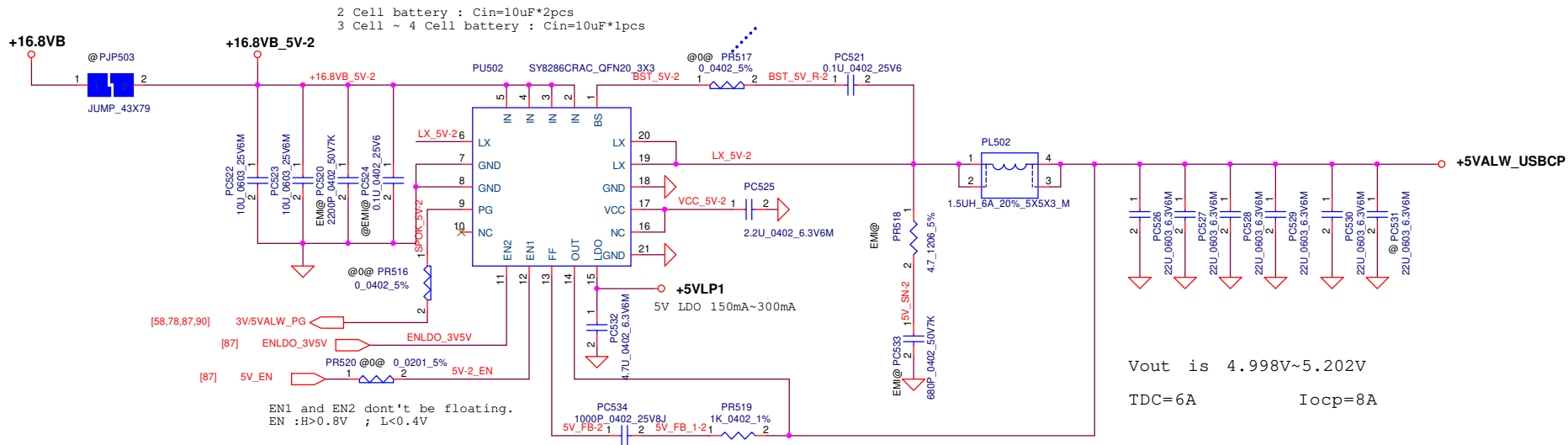


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Date: Thursday, July 30, 2020				Sheet 84 of 119		

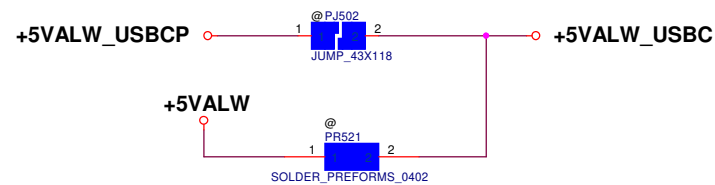




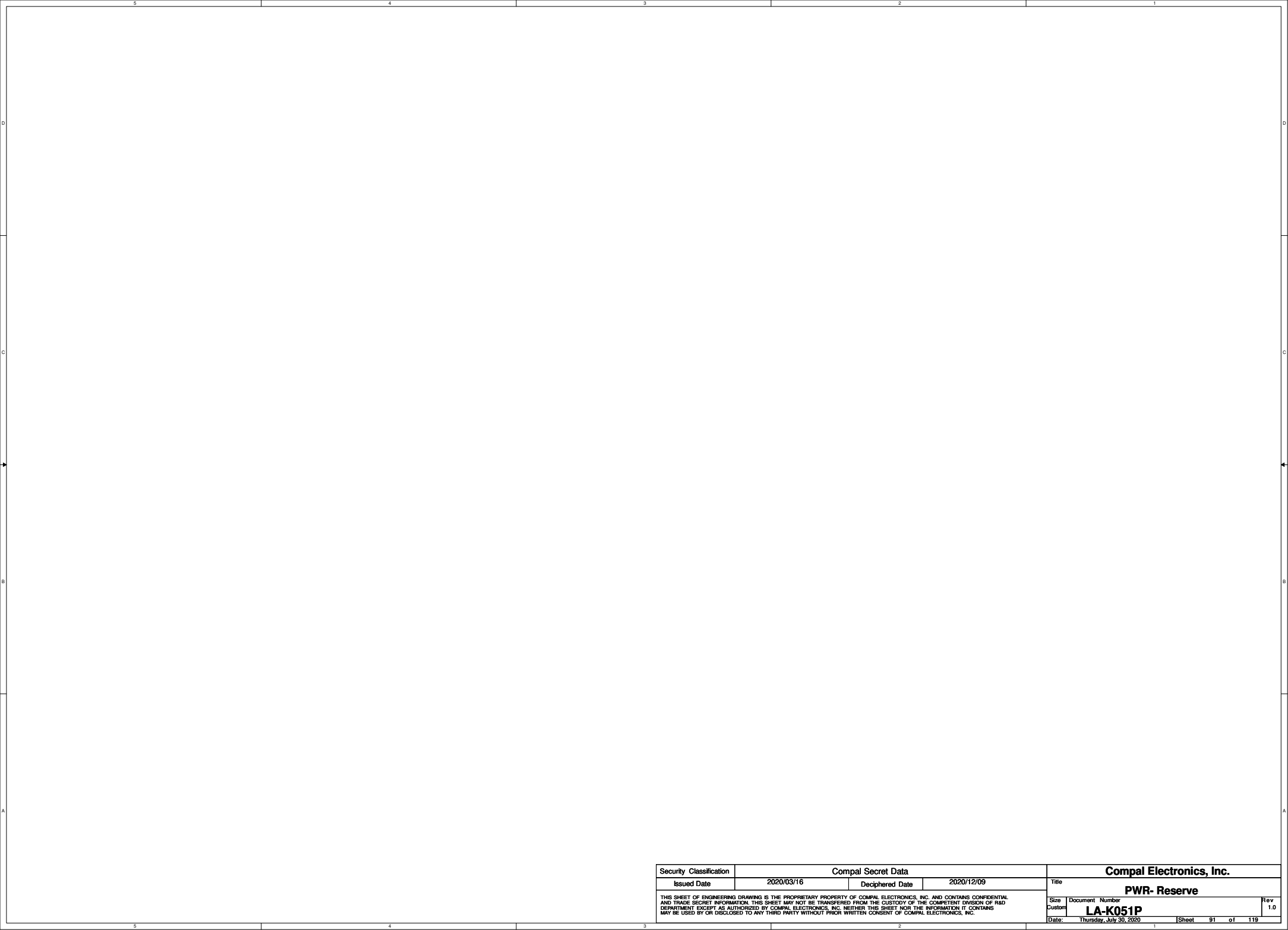
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				Size	Document Number
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Date: Thursday, July 30, 2020				Sheet	86 of 119
Rev		1.0			



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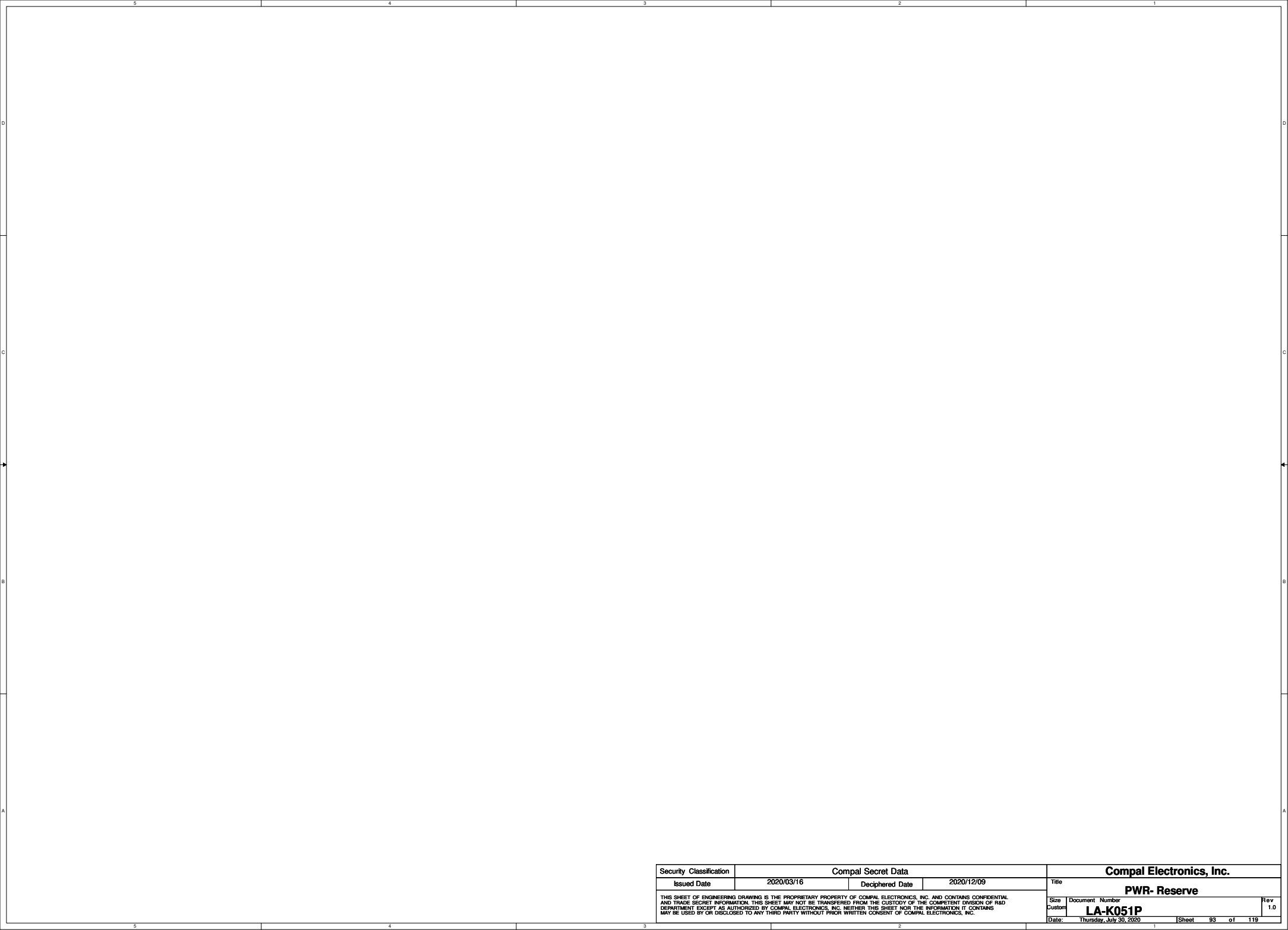
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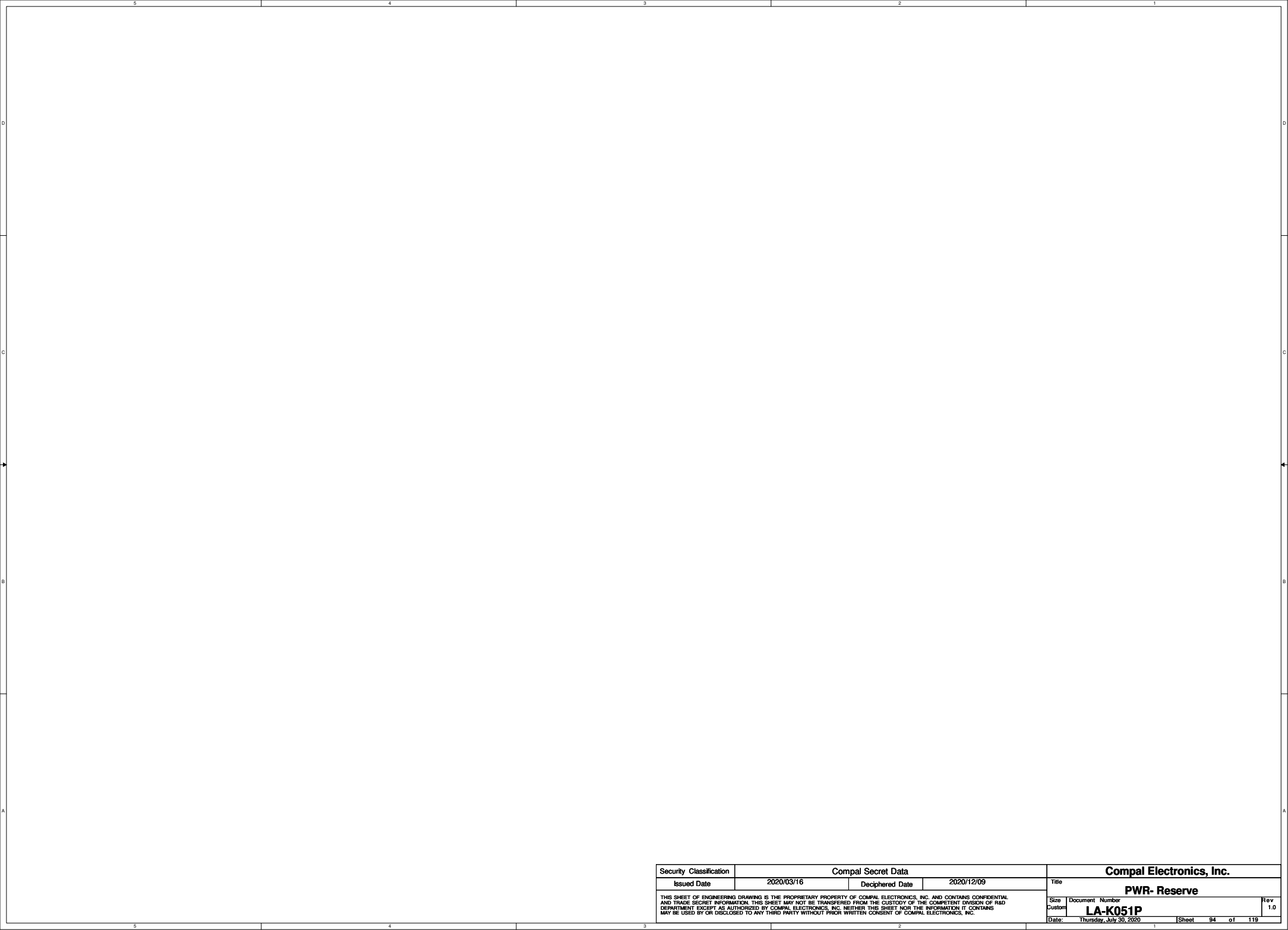
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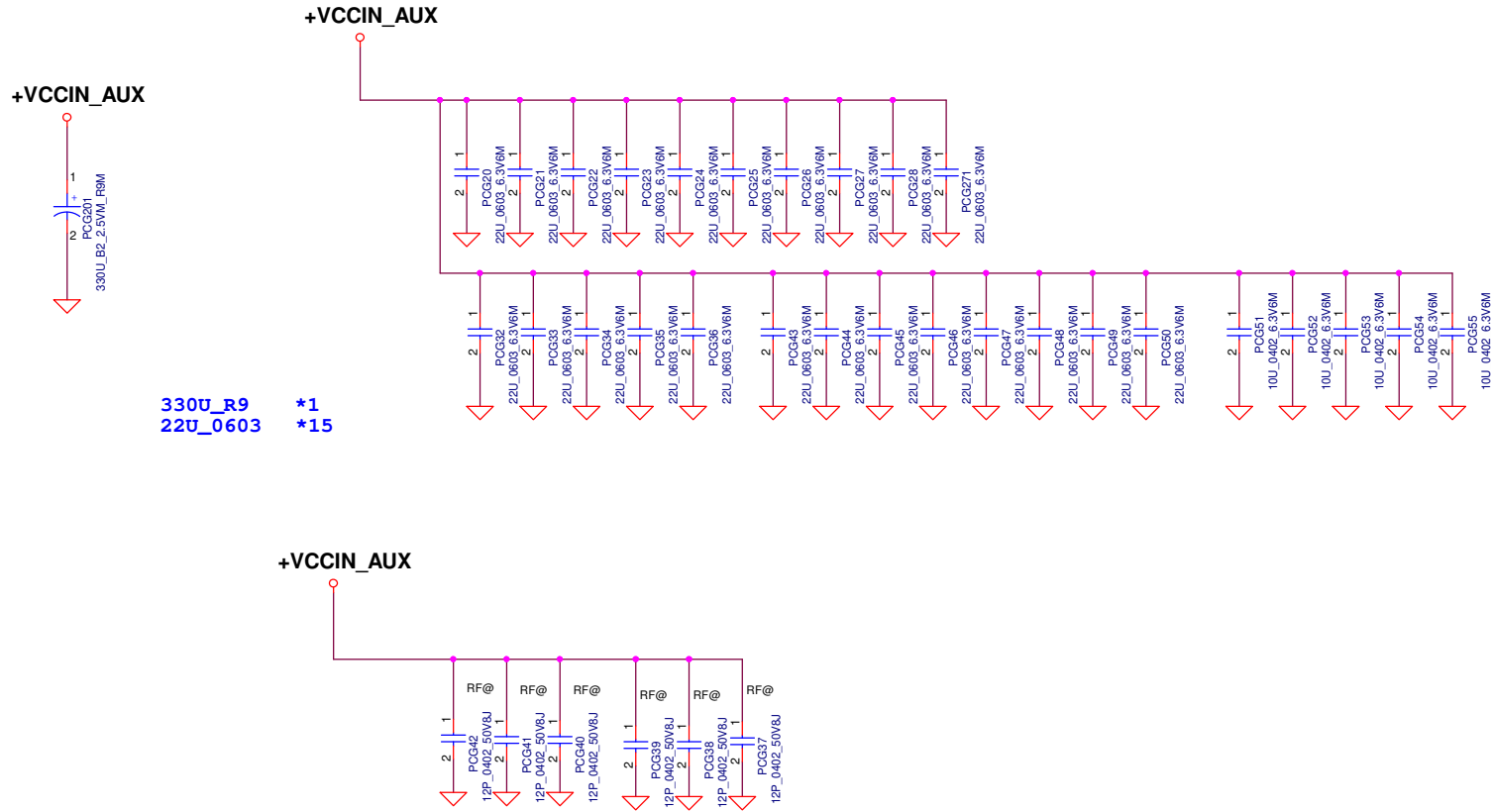
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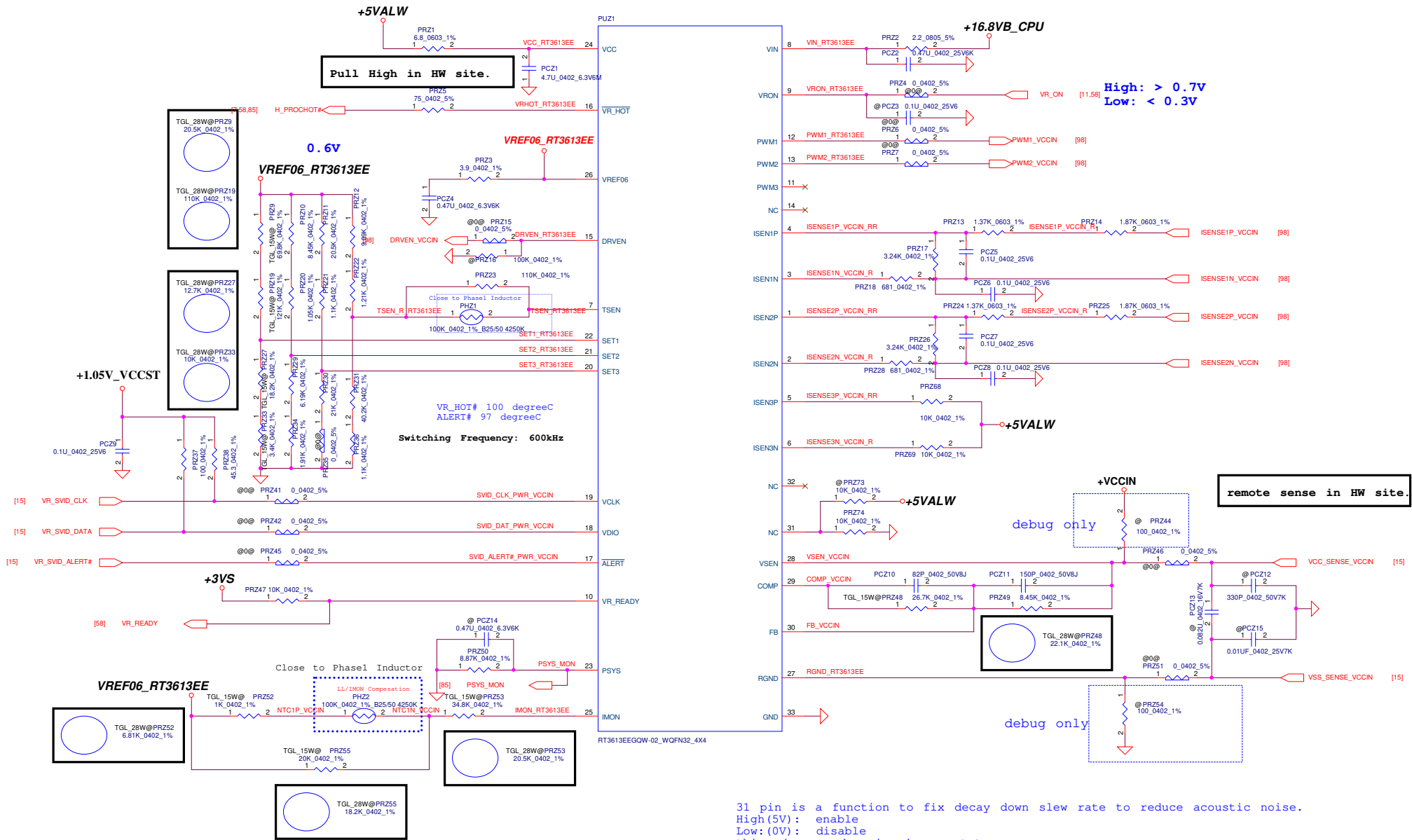
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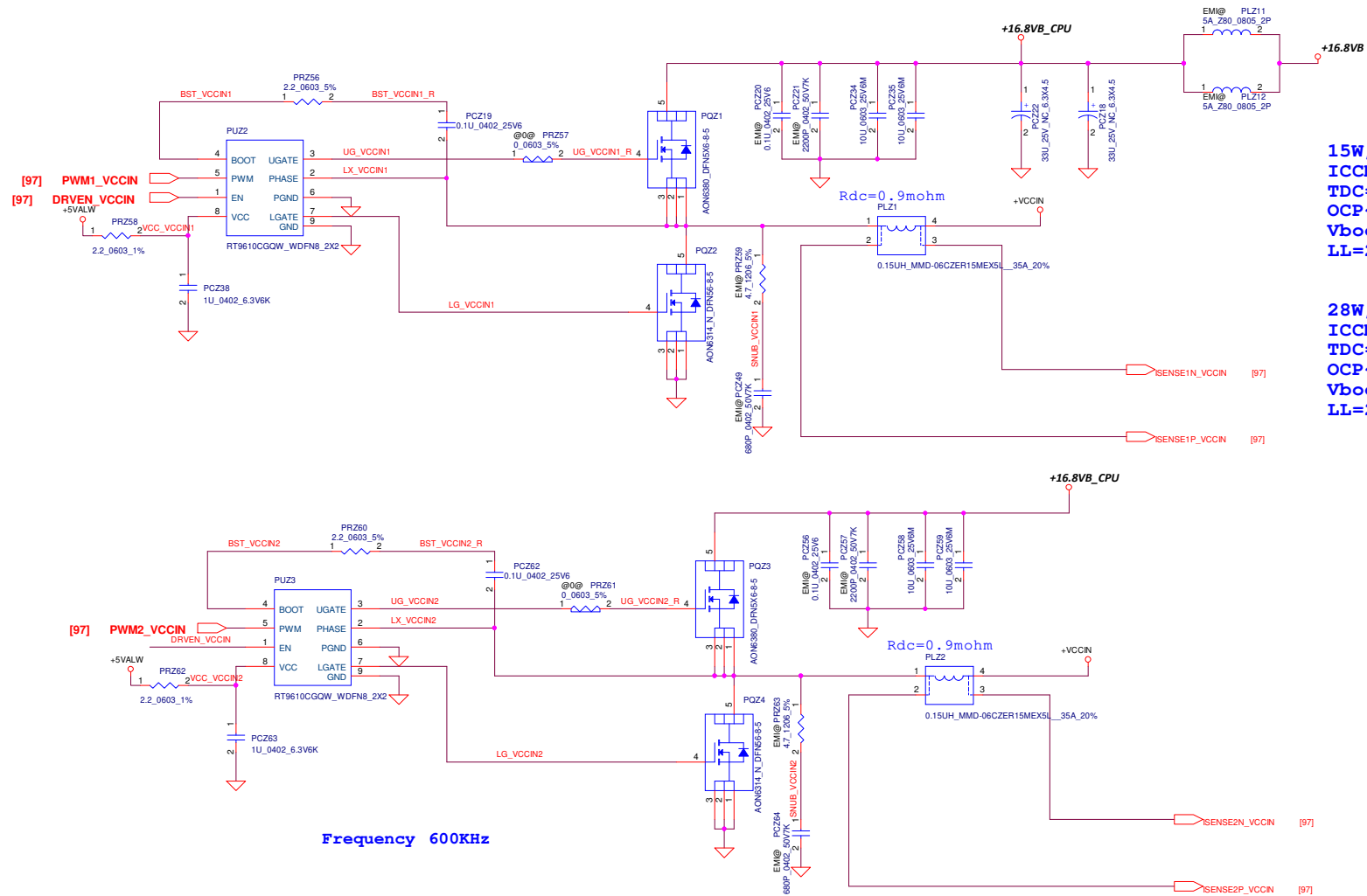
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				PWR- Reserve		
				Size	Document Number	Rev
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				Custom	LA-K051P	1.0
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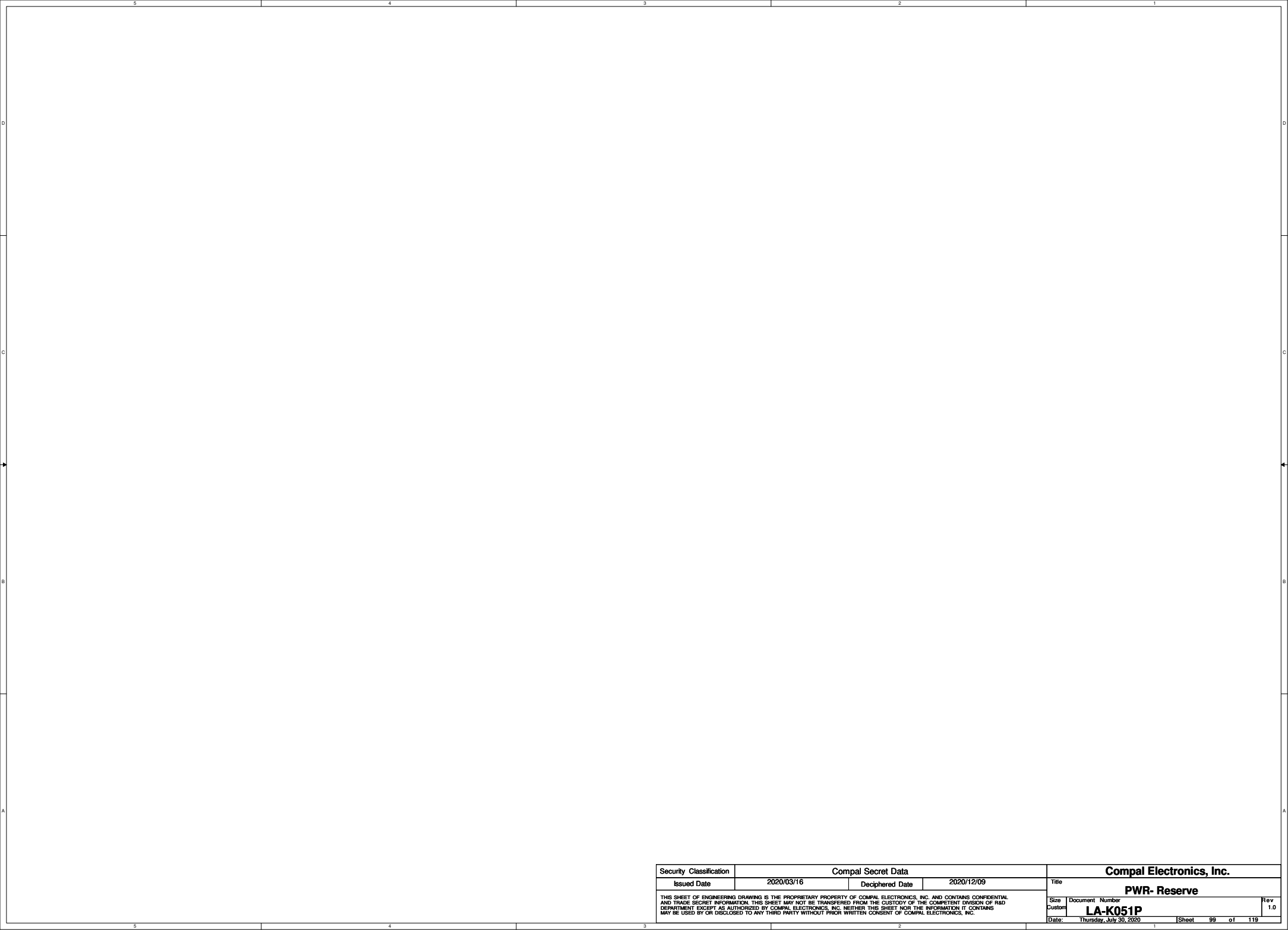


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				Custom	LA-K051P
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				Date	Thursday, July 30, 2020
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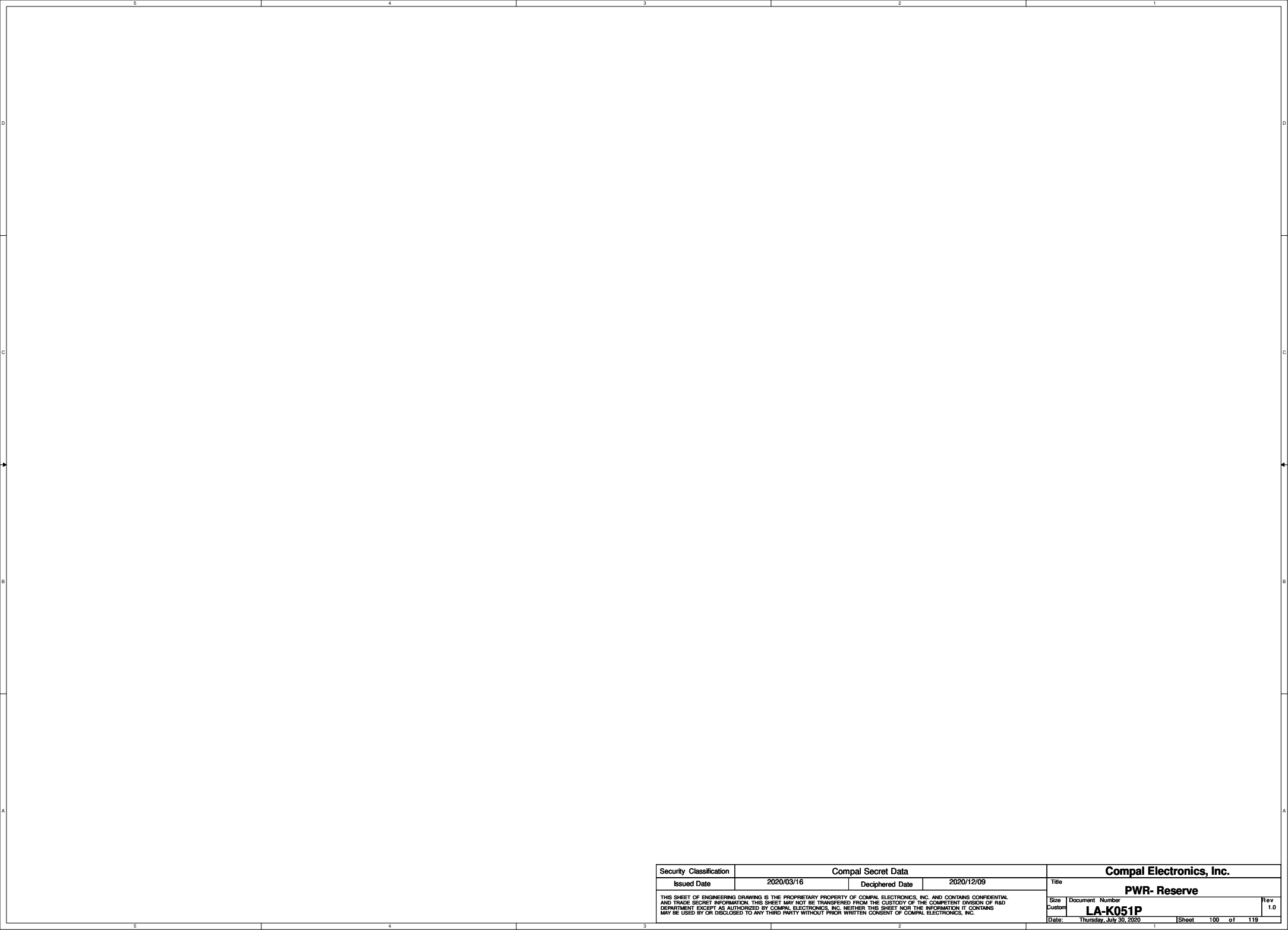


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 TDC=30A
 OCP~61.1A
 Vboot=1.8V
 LL=2mohm

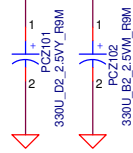
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 LL=2mohm



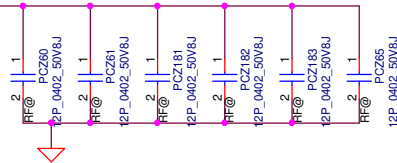
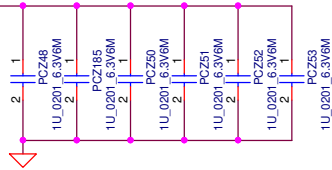
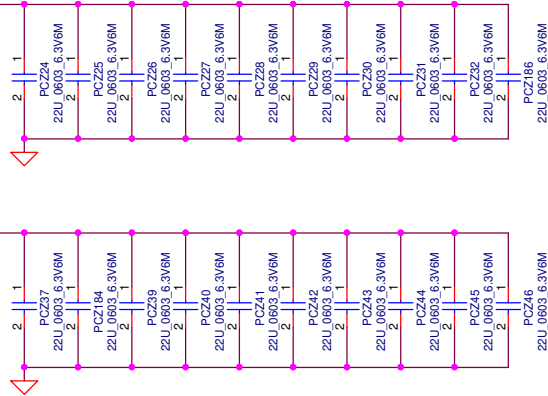
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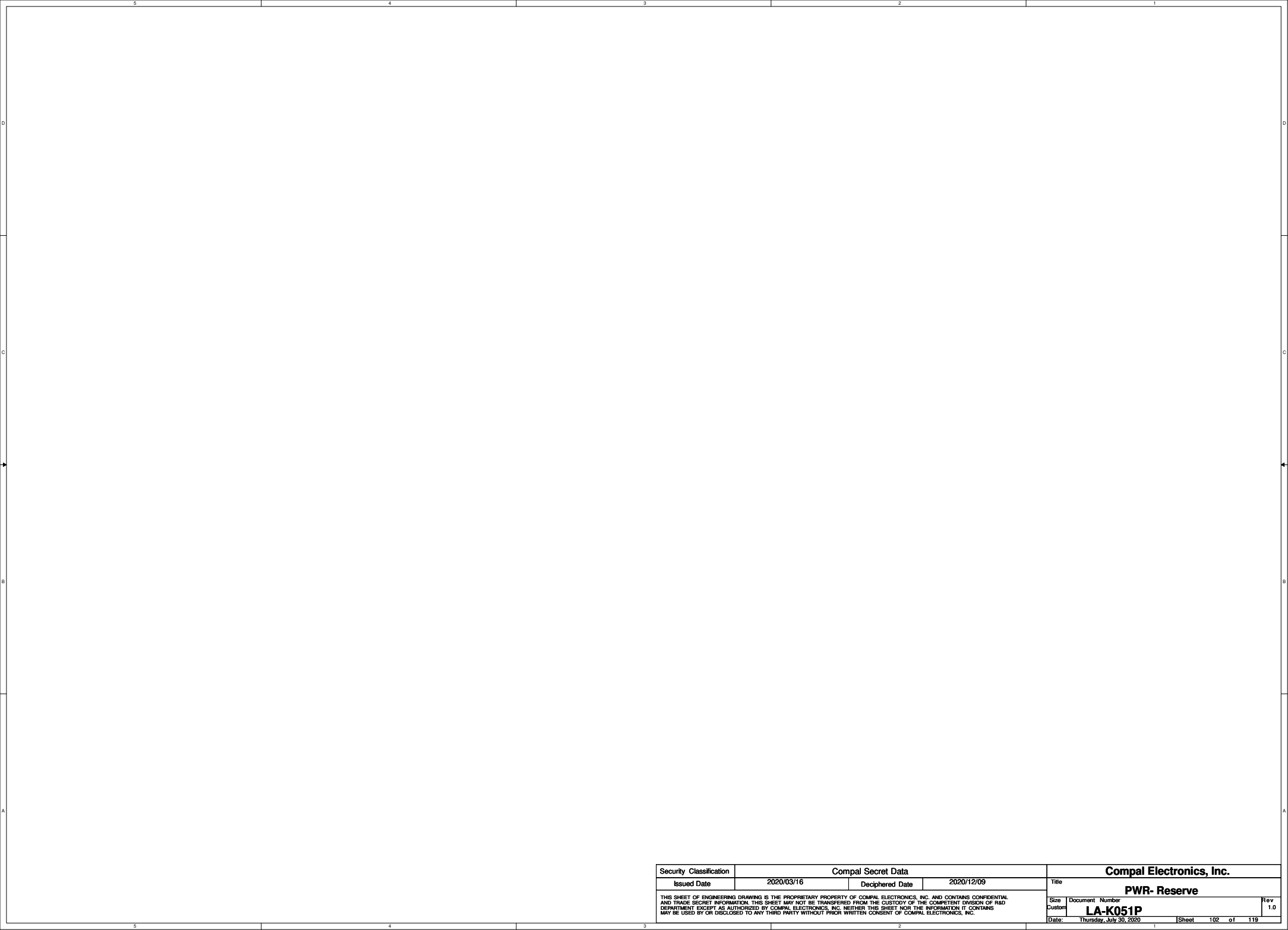
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Date: Thursday, July 30, 2020				Sheet	100	of 119



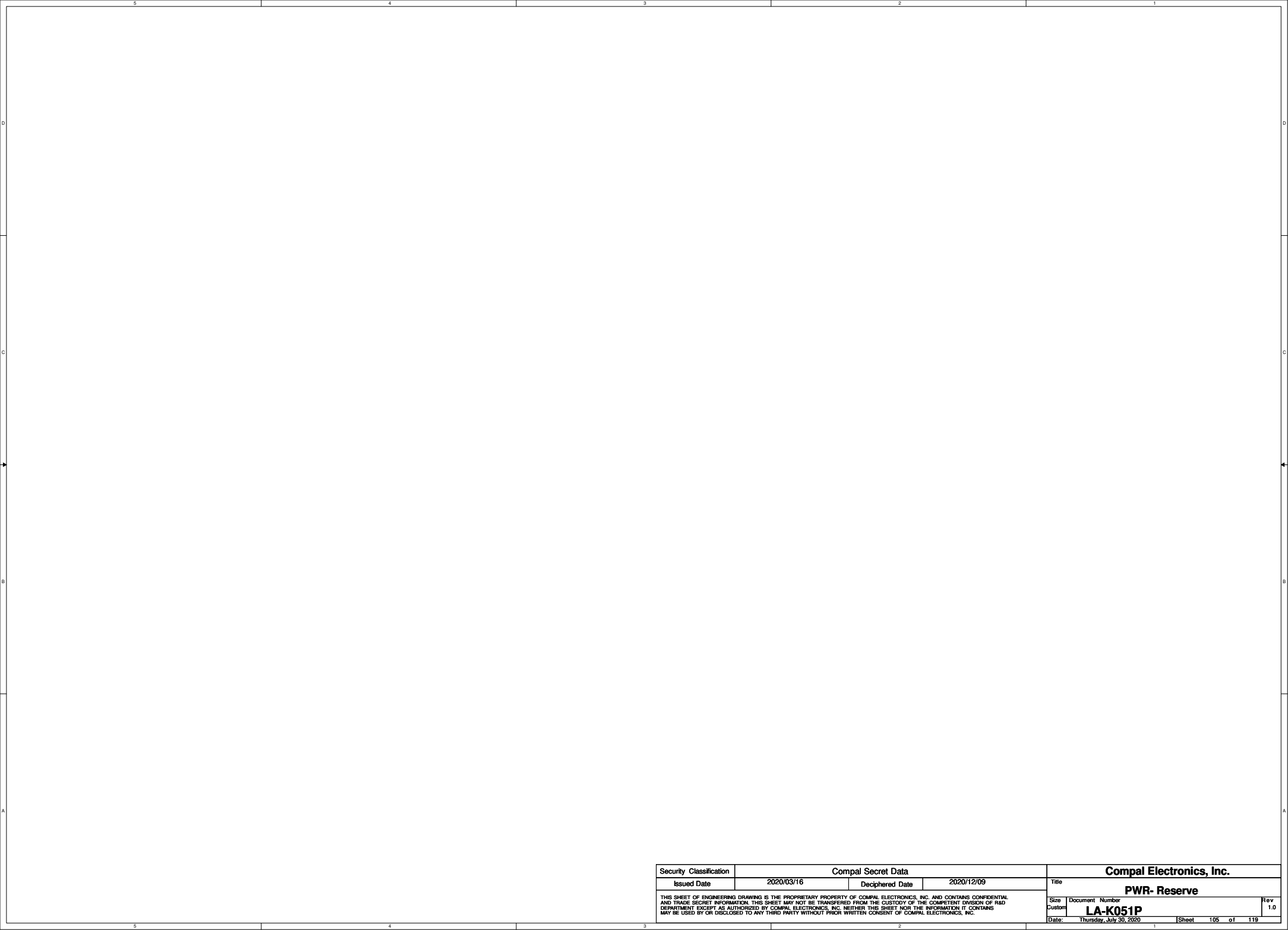
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330U_R9      *1
22U_0603     *18
1U_0201      *6
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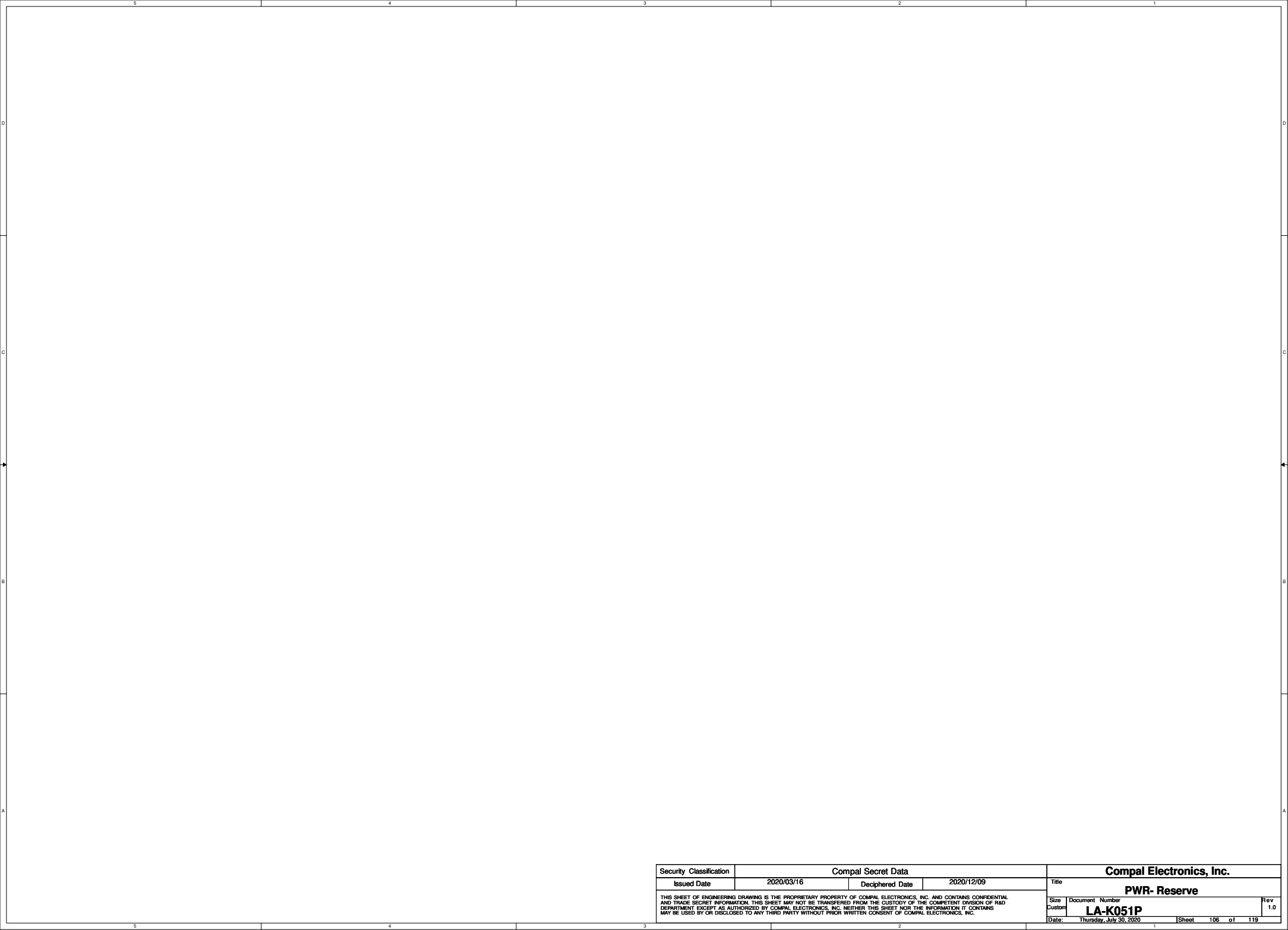
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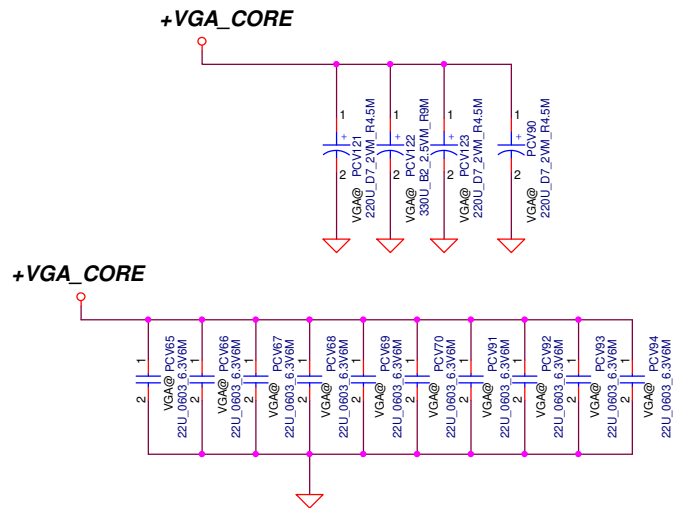
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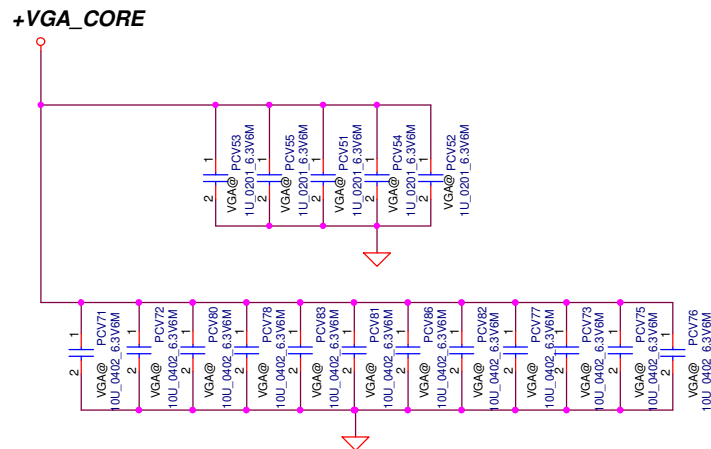


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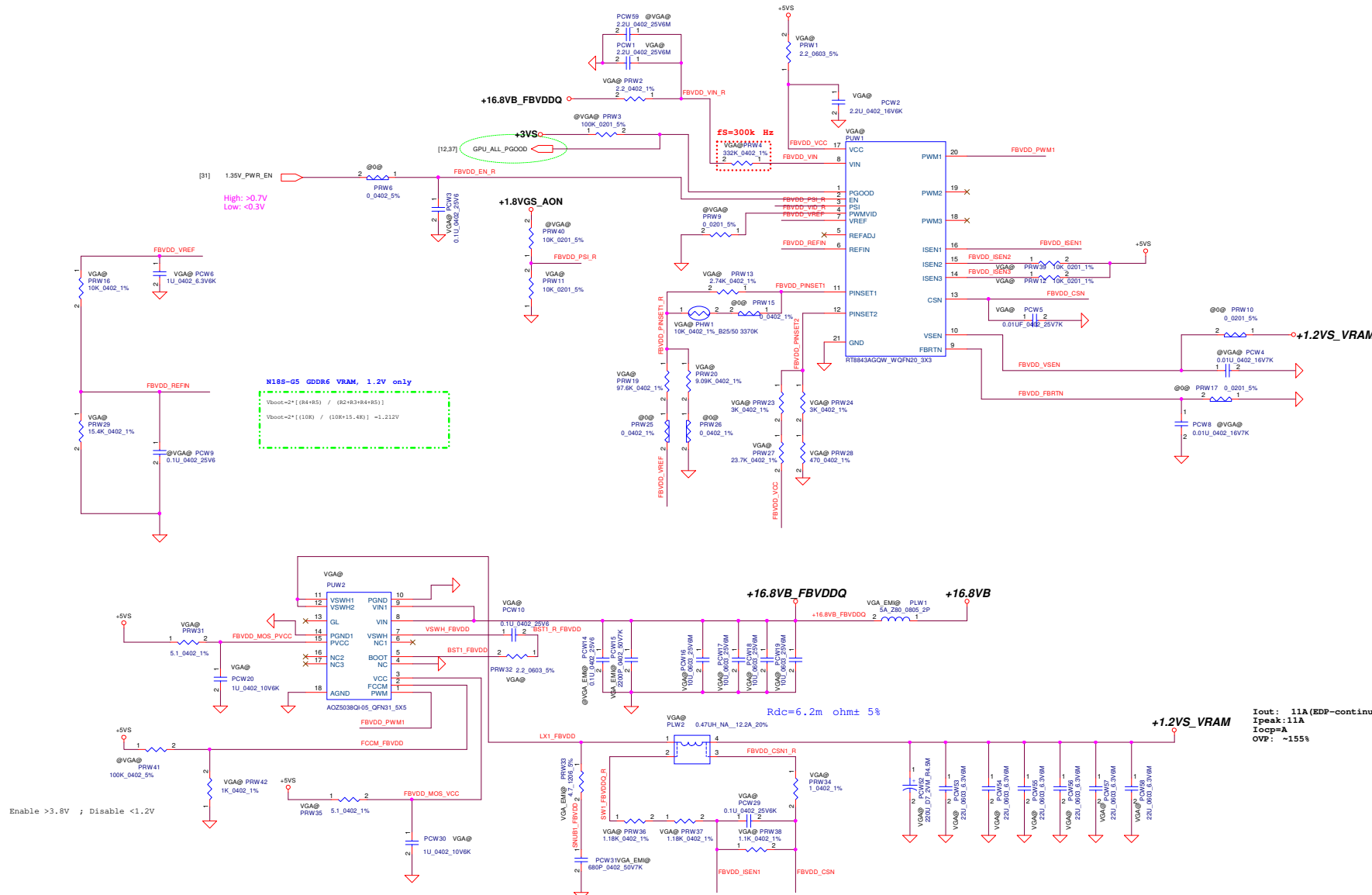


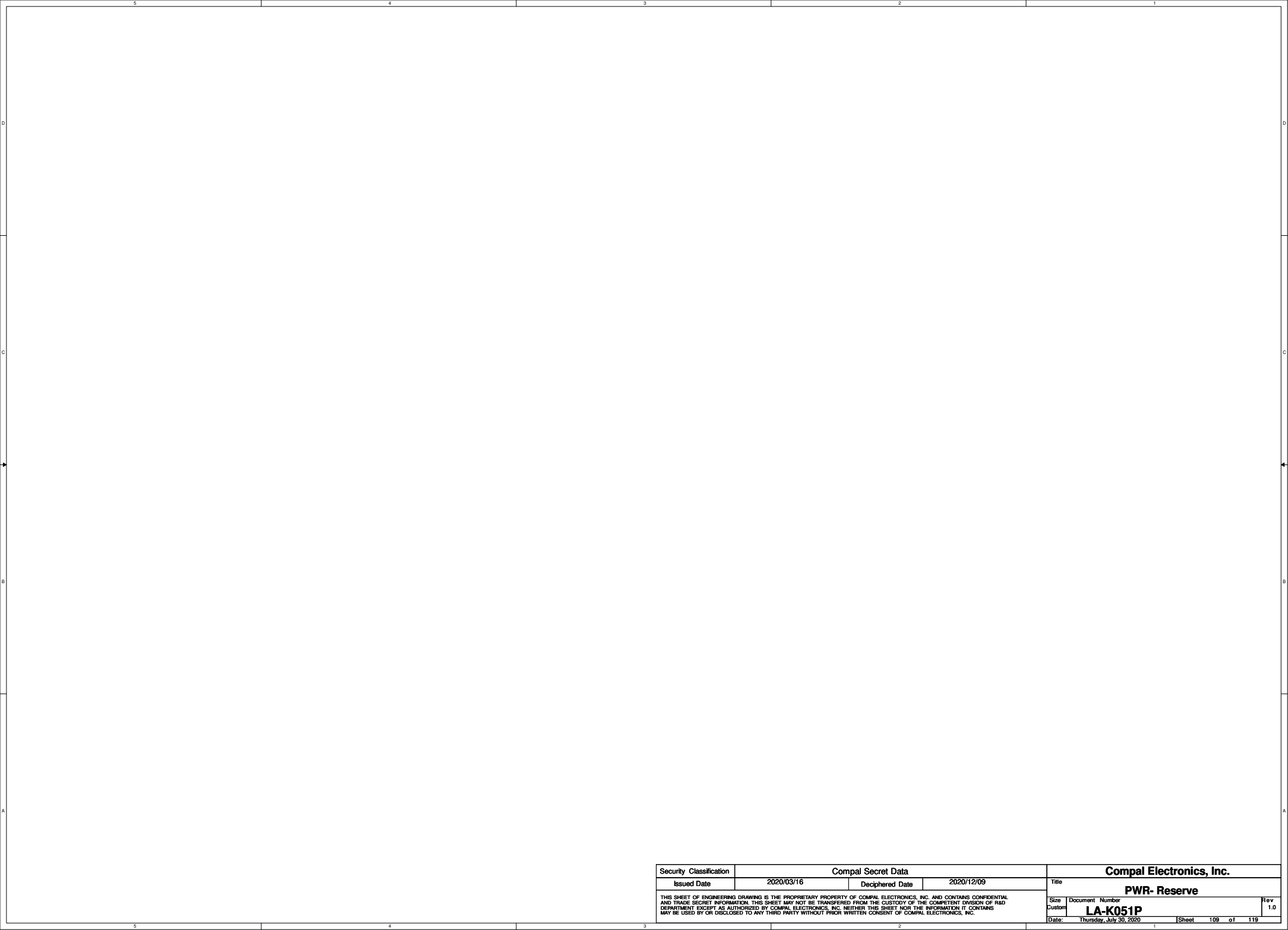
VGA_CORE output cap
330U_B2_2.5V 1pcs
220U_D7_2.5V 3pcs

22U_0603_6.3V 10pcs
10U_0603_6.3V 12pcs
10U_0402_16V 5pcs

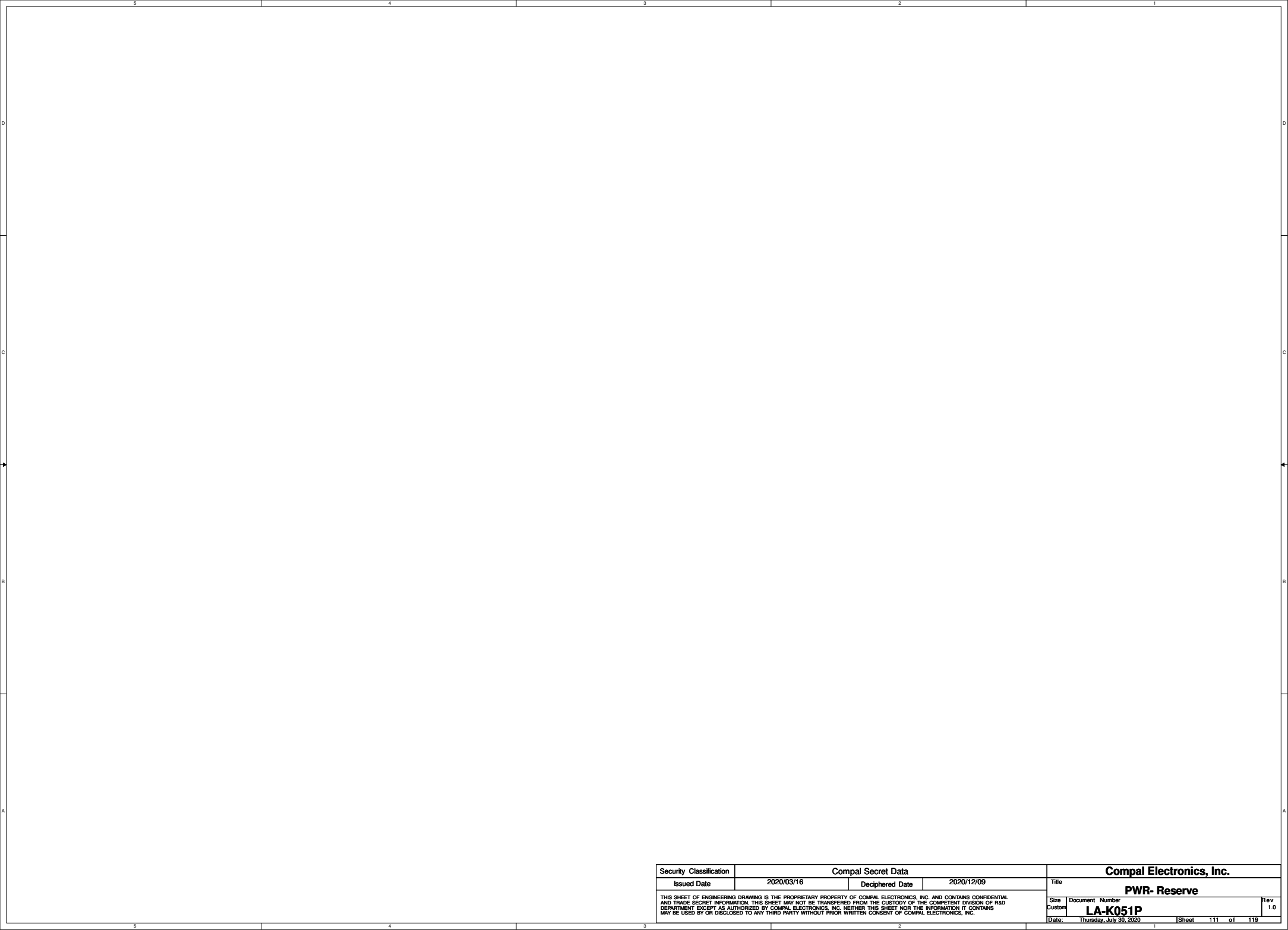


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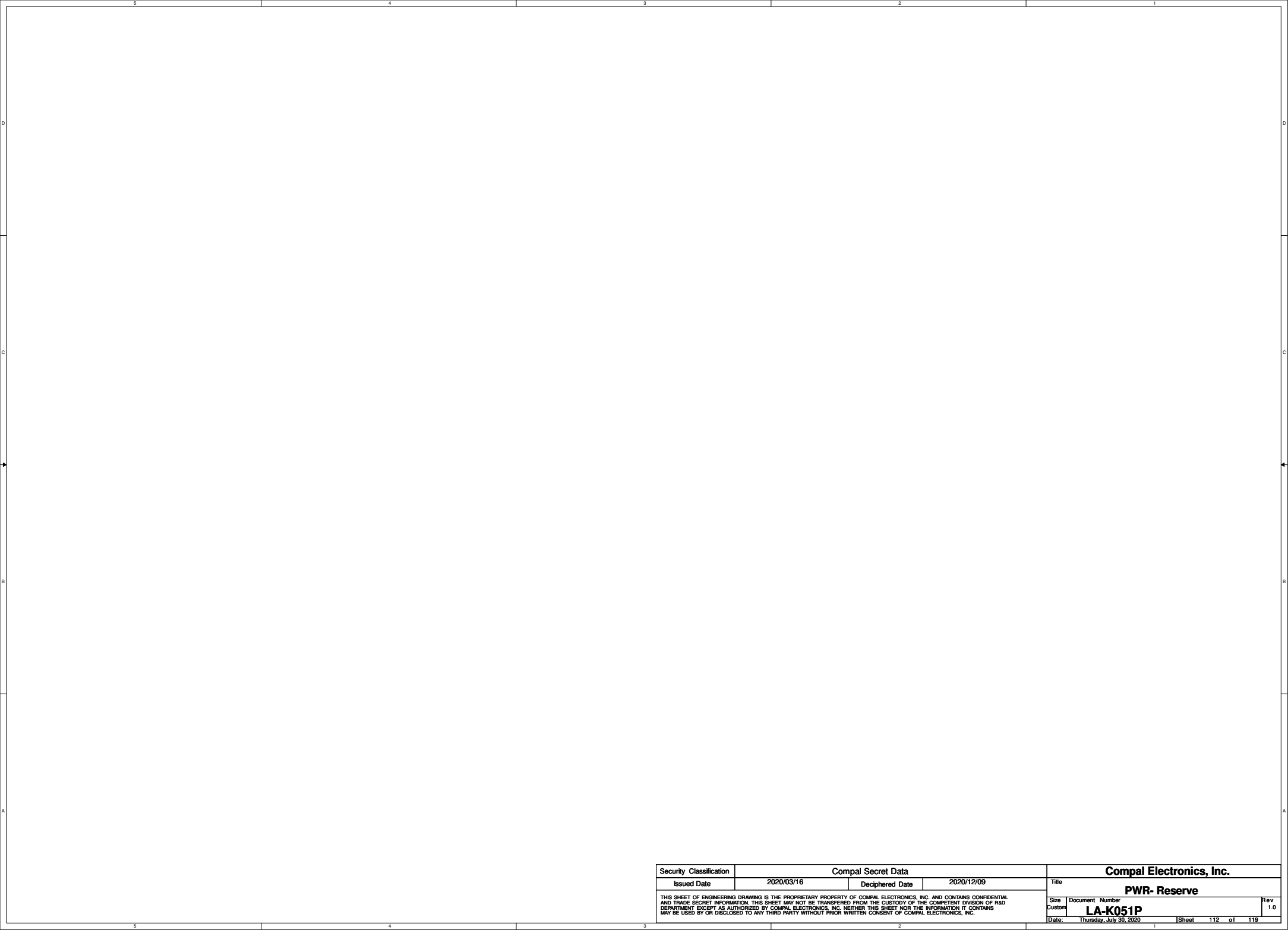




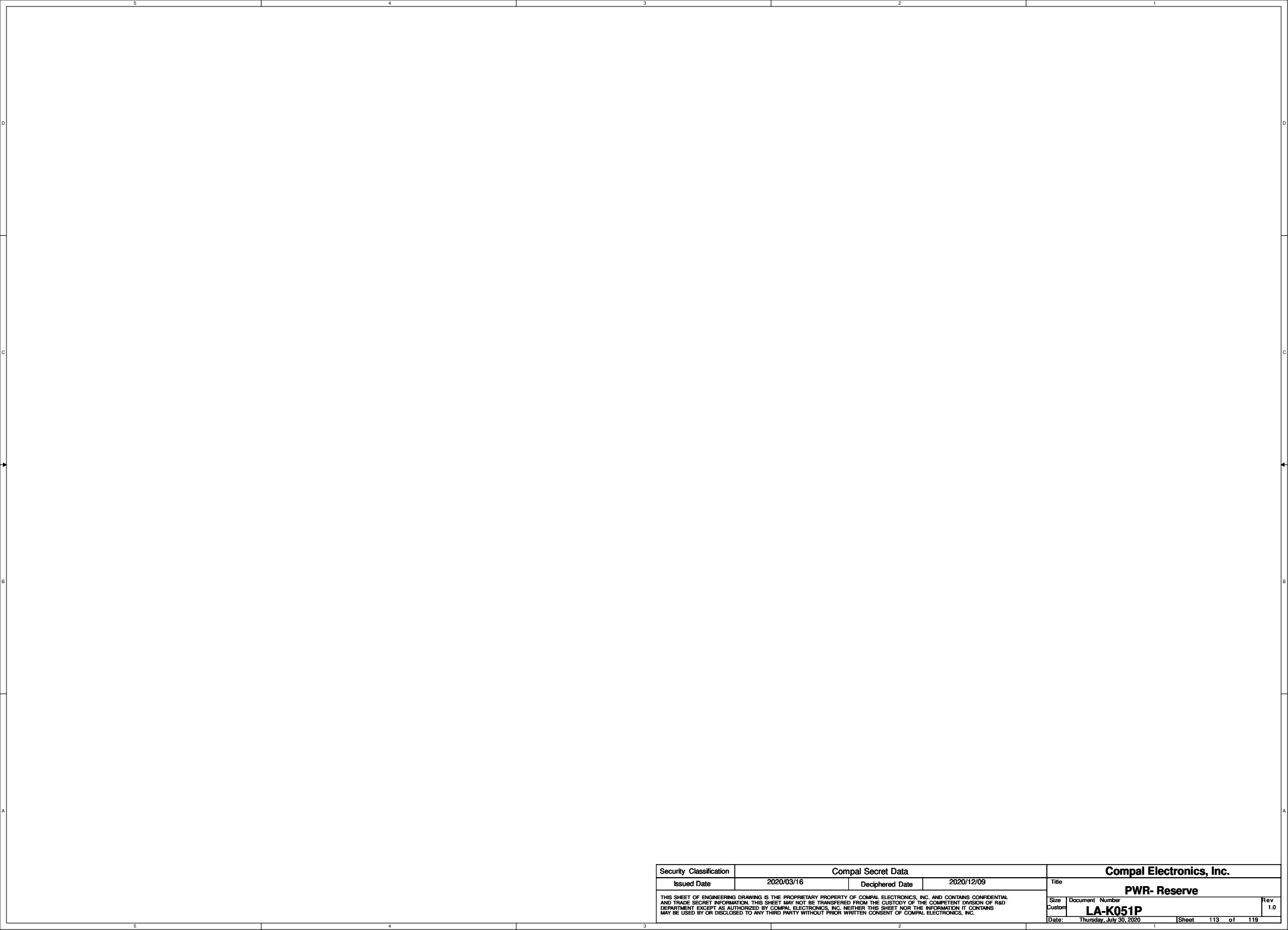
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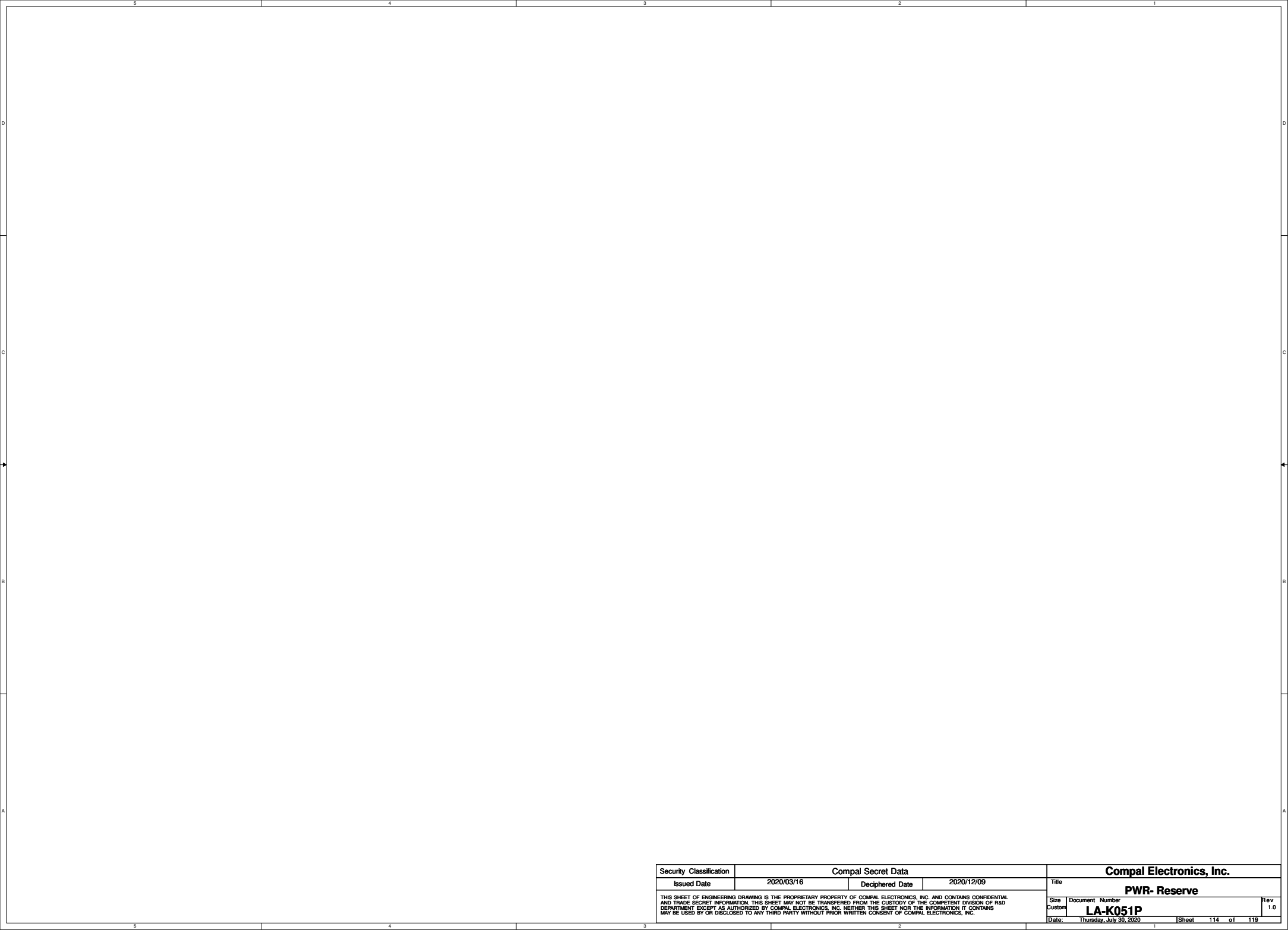
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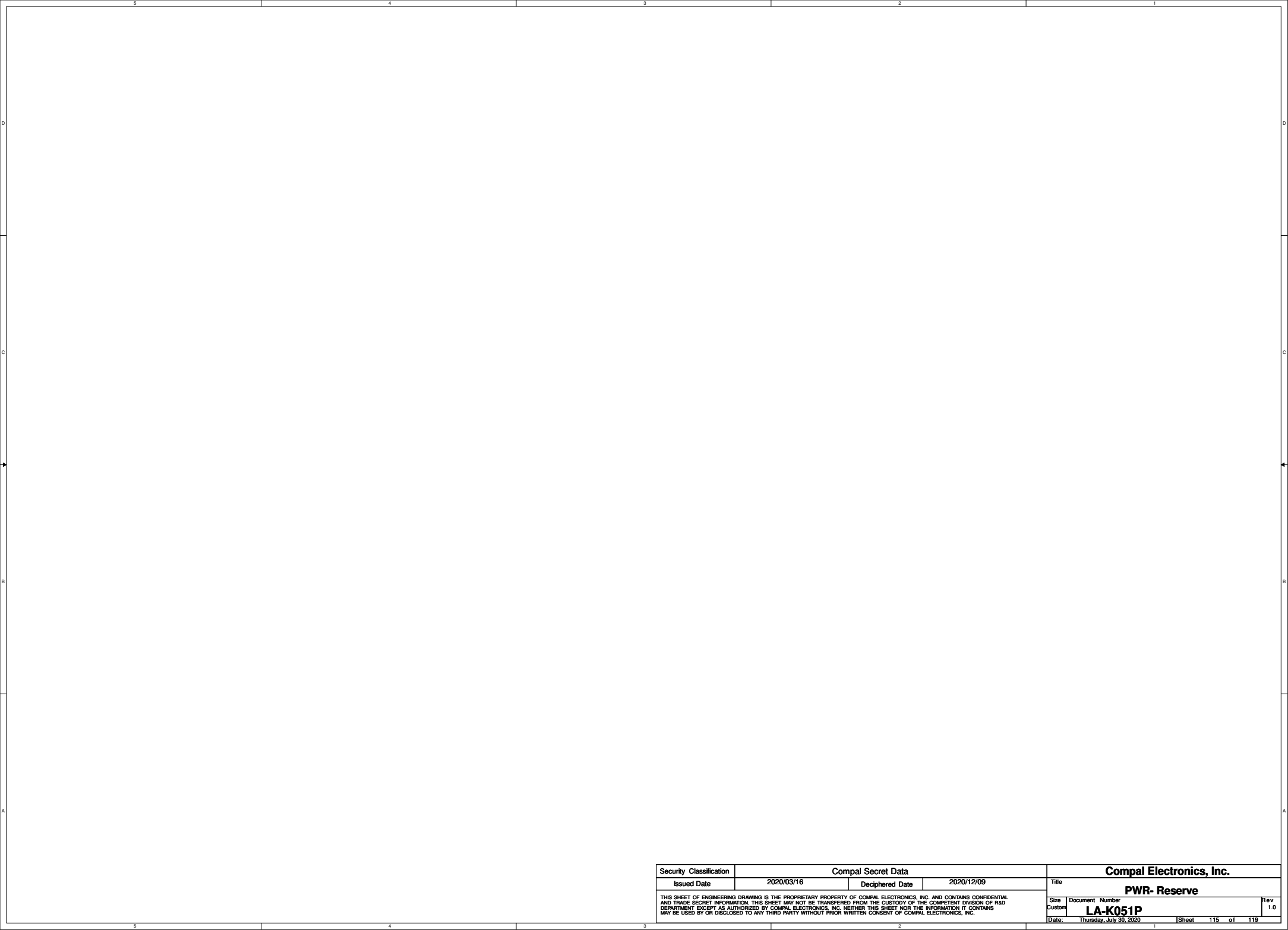
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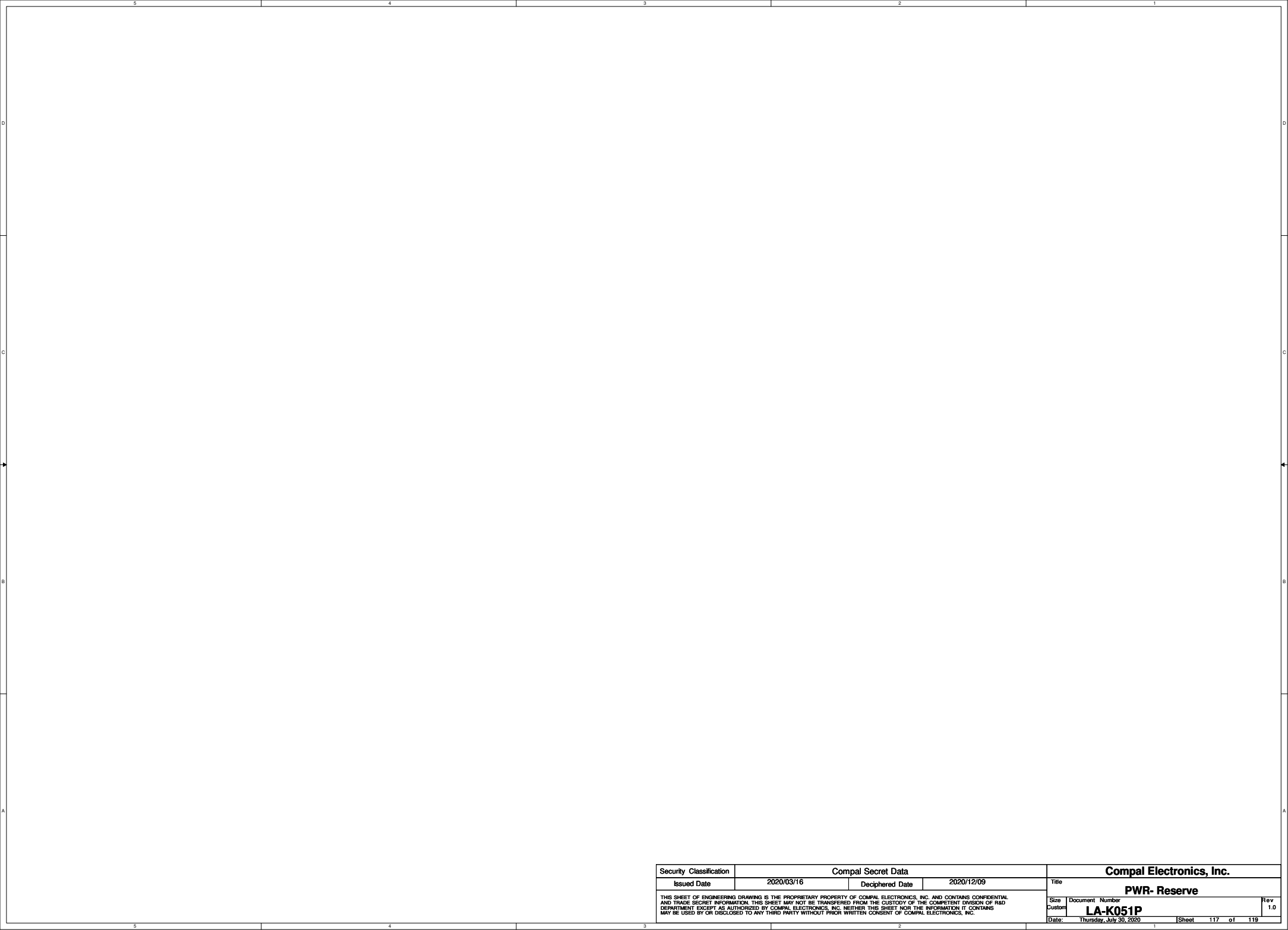
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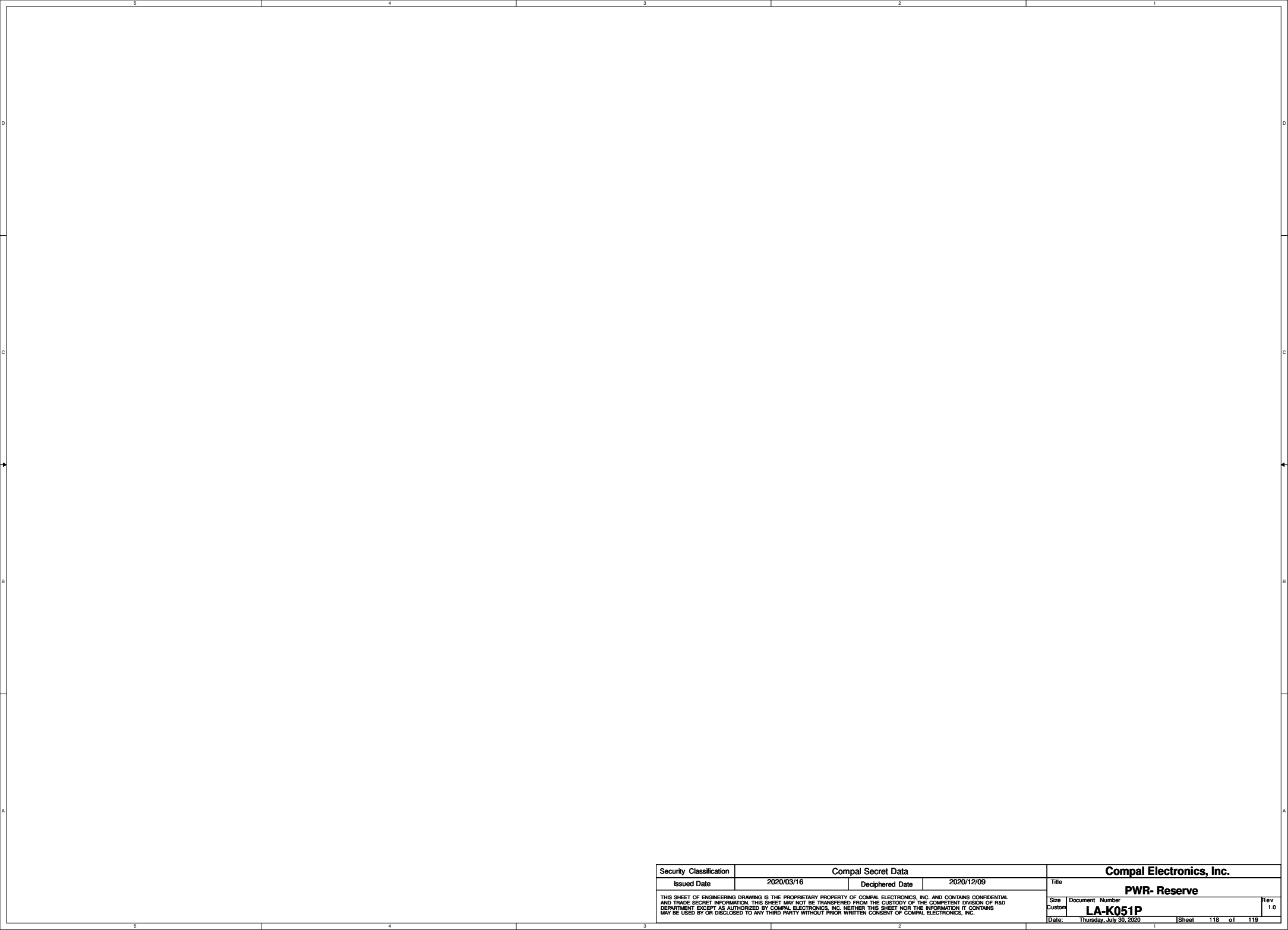
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Version change list (P.I.R. List)

Page 1 of 1 for
PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Change +1.2VS solution	108	Modify related component and circuit	0316A	FVT
2	change +5VALW_USBC enable signal	88	Add PR520 and connect to 5V_EN	0316A	FVT
3	Adjust AOZ5038 FCCM voltage level	104	Add PRV128 pull-high to +5VALWand PRV129 pull-down to GND.	0316A	FVT
4	Adjust +1.2VS_VRAM enable voltage level	103	Change PRV118 from 100K to 10K	0316A	FVT
5	Modify by CPU transient test result	97	Change PRZ48 from 23.2K to 22.1K Change PRZ52 from 2.49K to 6.81K Change PRZ53 from 28.7K to 20.5K	0323A	FVT
6	Request to pop by RF	96 101	Change PCG37,PCG38,PCG39,PCG40,PCG41,PCG42 to pop Change PCZ60,PCZ61,PCZ65,PCZ181,PCZ182,PCZ183 to pop	0328A	FVT
7	Reserve for +VCCIN_AUX output cap	96	Reserve PCG35,PCG36,PCG43,PCG44 22u_0603_6.3V	0328A	FVT
8	Request to pop by EMI	98	Change PCZ20,PCZ56 to pop Change PRZ59,PRZ63 to pop Change PCZ49,PCZ64 to pop	0328A	FVT
9	For power consumption	103	Change VCC pin connect from "+5VALW" to "+5VS"	0328A	FVT
10	change to pop by EMI request	85 87 88	PRB14,PRB15,PCB20,PCB21,PR502,PC513,PR518,PC533 change to pop	0410A	FVT
11	To adjust current limit value to 16A	108	Change PRW37 from 0 to 1.18K Change PRW19 from 118K to 97.6K Change PRW20 from 11K to 9.09K Change PRW27 from 2.43K to 23.7K Change PRW24 from 240 to 3K	0416B	FVT
12	Request by HW	95	change VCCIN_AUX_CORE_VID0_R to VCCIN_AUX_CORE_VID0 change VCCIN_AUX_CORE_VID1_R to VCCIN_AUX_CORE_VID1	0416B	FVT_
13	Request by HW	108	change from "+1.35VGS_PGOOD" to "GPU_ALL_PGOOD"	0416B	FVT_
14	For test point adding requirement	88	change PR520 from 0402 to 0201 size	0416B	FVT_
15	To optimize SMT process	82 95 85 97 87 98	change from 0 ohm to short-pad : PR8,PRB4,PRB11,PRB32,PRB10,PRB12, PR511,PRG2,PRG5,PRG12,PRG14,PRG27,PRG30,PRG6,PRZ6,PRZ7,PRZ46, PRZ51,PRZ41,PRZ42,PRZ45,PRZ35,PRZ15,PRZ57,PRZ61	0416B	FVT_
16	To optimize SMT process	89 103 90 108 95 110 97	change from 0 ohm to short-pad : PRM3,PRM4,PR251,PR1804,PRG11,PRZ4,PRV10,PRW6,PRE1	0525A	SIT
17	NV request to smooth undershoot/overshoot during VID change	103	PCV16 change to 4700p	0525A	SIT
18	For sequence tuning	103	PCV20 change to unpop	0525A	SIT
19					
20					
21					
22					
23					

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		Deciphered Date		2020/12/09	
				PWR- PIR (1/2)	
				Rev 1.0	
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